DESIGN AND SIMULATION OF FUNCTIONAL CELLS FOR MOS LSI SYSTEMS

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By
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to the

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CERTIFICATE

It is to certify that this work entitled "DESIGN AND SIMULATION OF FUNCTIONAL CELLS FOR MOS LSI SYSTEMS" by E.R. Sheikh has been carried out under my supervision and this work has not been submitted elsewhere for the award of a degree.

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To,

My Parents

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E.R. Sheikh

ABSTRACT

Since the development of small-scale integrated circuits the density of components on an IC chip is continuously increasing As the level of integration increases the design complexity also increases rapidly. A large amount of effort will be required to put into design such large scale integrated systems. A systematic approach is to break the task of complete design into manageable subtasks of cell design. We have restricted ourself to design and analysis of such subcircuits or cells.

After functional specification of the cell, next step is to design the logic to achieve the functional relationship between input and output. Various representative examples, in combinatorial sequential, static/dynamic, ratioed /ratioless logics have been presented using random and structured approaches of logic design. Layout for some of the functional cells have been prepared and the circuits have been simulated using SPICE including the effects or parasitics. Values of parasitics have been evaluated from the cell layout. Device models for circuit simulation have also been included and an interactive program is developed for the extraction of MOSFET model parameters for CAD applications.

CONTENTS

CHAPTER 1

INTRODUCTION

The silicon integrated circuit technology is evolving continuously towards smaller devices and denser, and more complex functions on each single silicon chip. Successful design and fabrication of circuits, containing 500 thousand transistors on a single chip has already been reported. It is expected that by the end of this decade it will be possible to have one million transistors on a single chip [1]. As the level of integration increases the design complexity also increases rapidly. A large amount of effort will be required to put into design such large scale integrated systems. A systematic approach is to break the task of complete design into manageable subtasks of cell design [2]. Each subtask can then be performed separately with no need to consider more than one subtask at a time.

Scope of this thesis is limited to complete design and analysis of such subcircuits or cells, which is to be used in LSI/VLSI systems. A number of design methods are available for design of logic circuits, namely, random logic, gate array, transistor switch array, programmable logic array etc. All these methods have been discussed in detail in the following chapters using illustrative examples. Computer simulation for analysis and verification of design, is necessary at each phase of design. Extensive use of simulation program SPICE is

made during all designs included in the thesis. Also a computer program is developed to perform transient analysis of MOS circuit. In the subsequent paragraphs we will present brief discussion on the contents of each chapters.

Chapter 2, starts with description of basic structure of MOS device and its I_D-V_{DS} characteristic. Then higher order effects have been discussed and some semi-empirical relations have been presented to take these effects into account. To build the concepts of MOS logic circuits, a E/D inverter is analysed in detail. Choice of W/L ratio and effect of capacitive load on rise-time and fall-time (i.e. total signal delay) has been considered. The concepts of inverter circuit is then extended to analysis of NOR and NAND gates. During rest part of this chapter, DC and Transient analysis of the MOS circuits have been discussed. For analysis of larger circuits computer aids are inevitable. A transient simulation algorithm and a program based on this algorithm have been described. Chapter concludes with a discussion on the results of transient analysis of three circuits of inverter, NOR and NAND gates, obtained by using our program SIMIC.

Chapter 3 - In this chapter MOS IC design methodology has been described in detail. Exclusive-OR circuit is designed in Random logic, it's stick diagram and detailed layout also has been prepared. As an example of design of PLA, one bit full

adder has been implemented and complete layout is prepared. Performance of the circuit is verified by transient analysis on SPICE. To consider the dynamic logic, we have designed a dynamic two-phase ratioless shift register. Layout of this circuit is also prepared and performance is analysed using SPICE. Principles of design of sequential logic is discussed using an illustrative example of 4-bit variable modulo counter (Reset to control-data input). Design of this variable modulo counter is based on PLA. Design of PLA feedback ensures spike-free, synchronous operation during counting. Chapter is concluded with circuit design. In this, design of full adders shift register, counters and memories have been discussed.

Chapter 4 - SPICE is a commonly used circuit simulation program. We have also used it extensively in our work, and we have included discussion on that part of SPICE which is relevant to MOS circuits. MOSFET models used in the SPICE have also been discussed. One can easily understand that to use the SPICE effectively one should know the process and geometrical parameters of device. Also accurate estimation of parasitic capacitances and resistances is very important for correct transient simulation. A computer program is developed which works interactively to extract the parameters of MOSFET model for use in SPICE simulation.

Chapter 5 - In this chapter discussions and conclusions of the thesis have been presented.

CHAPTER 2

MOS CIRCUITS

In this chapter we will review the basic concepts or MOS transistor operation both qualitatively and quantitatively. During this we will consider I_D-V_D relationship of first order only. We will then design and analyse the basic building blocks of MOS logic circuits. We will consider MOS inverter (E/D and CMOS) NOR and NAND gates. Effect of load capacitance on signal delay is also considered. Circuit simulation at device level is necessary to predict the electrical behaviour of the circuit before actually fabricating it. Computer simulation programs essentially uses models (a set of mathematical equations describing the terminal behaviour) for representing the behaviour of the device over its full operating range. A MOSFET model for computer-aided analysis which takes some prominent effects into account has been derived. And a computer program is developed using this model for transient analysis. Results of transient analysis of inverter, NOR and NAND gates have been discussed at the end.

2.1 MOSFET CHARACTERISTICS

MOS transistors are unipolar devices. A common structure of MOS transistor is shown in Fig. 2.1. Bulk semiconductor for N channel MOS(referred as NMOS) is P-type and that for P channel

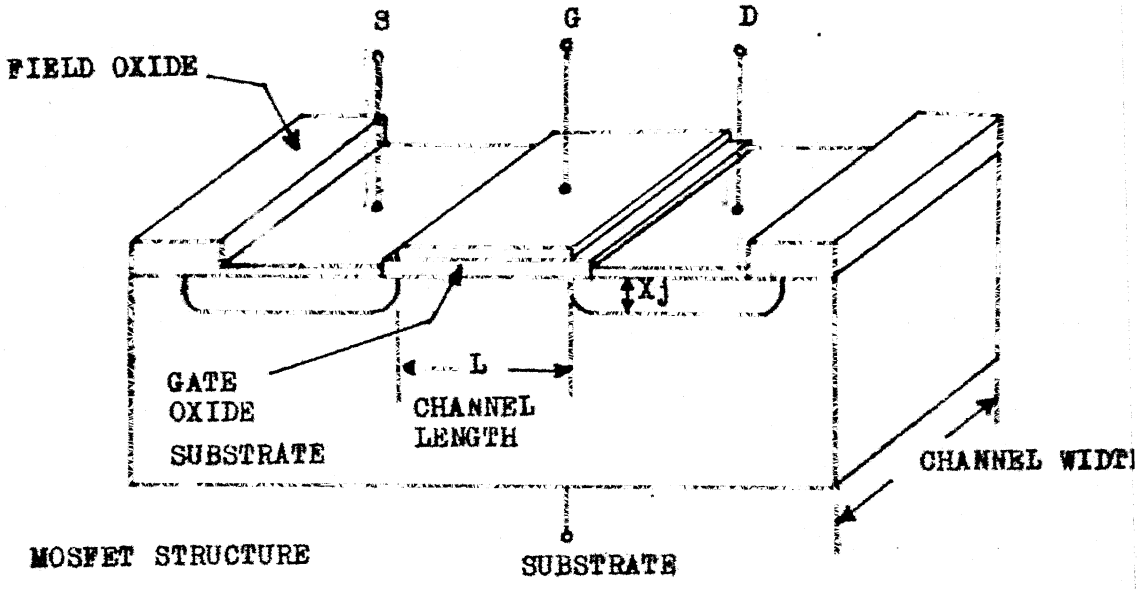


FIG. 2.1 MOSFET STRUCTURE

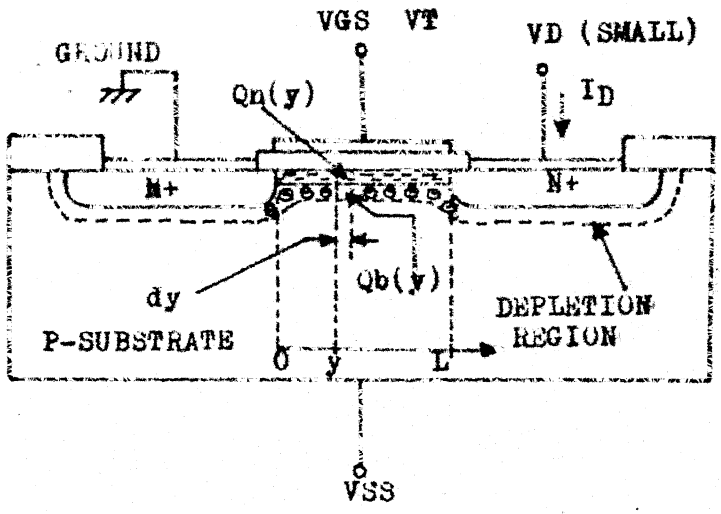


FIG. 2.2 N. CHANNEL MOSFET AT THE VERGE OF CONDUCTION

MOS (referred as PMOS) is N type. In an NMOS devices as shown in Fig. 2.2 , two heavily doped N^+ regions are referred as drain and source. Heavily doped polysilicon layer is deposited over the thin gate oxide layer. The basic device parameters are the channel length L ; the channel width W ; the oxide thickness t_{OX} : the junction depth X_j; and the substrate (bulk) doping N_A. NMOS device is preferred over PMOS device because the current carriers in NMOS (i.e. electrons) exhibit higher mobility than that of the PMOS, it offers higher gain and speed.

2.1.1 MOS Transistor Operation [4]

In an N-channel MOSFET, when no voltage is applied to the gate, the source-to-drain regions corresponds to two $P\text{-}N^+$ junctions connected to back to back. In this situation only reverse saturation current can flow through drain to source (which is very small of the order of 10^{-14} Amp). When a positive gate potential is applied (with respect to the substrate,source and substrate grounded together), it will induce electrostatically a negative charge on the substrate and will repell holes thus depleting the channel region for majority carriers. If an increasingly large voltage is applied at the gate then more and more electrons will be attracted towards the surface. Eventually the electron density locally near the surface exceeds the hole density and a conducting channel of electrons from drain to source is formed, through which a large

current can flow. This condition is called inversion of the semiconductor below the thin oxide. The gate voltage which is necessary to cause inversion and to form a channel is called threshold voltage of the device. The conductance of the channel can be modulated by varying the gate voltage. Higher order effects on the conductance of the channel will be discussed later.

MOS transistors are referred to as enhancement or depletion type depending whether or not a conducting channel exist between drain and source at zero gate bias. If a channel exists at $V_G = 0$ then it is a depletion type transistor otherwise enhancement type.

2.1.2 Drain Current Equations [4,6]

Application of gate voltage in excess of threshold voltage forms a conducting channel from drain to source. Current through the channel (drain current) is proportional to drain-source bias, V_{DS}, when V_{DS} is small. As the drain voltage increases, it eventually reaches a point at which the channel depth X_i at drain end is reduced to zero ; this is called pinch-off point and corresponding drain-source voltage is called V_{DSSAT}. Beyond this point drain current remains essentially the same because potential at the drain end of the channel remains the same, V_{DSSAT}.

We shall now derive the basic MOSFET characteristics under the following idealized conditions : (1) There are no interface states present near the surface ; (2) Only drift current dominates ; (3) carrier mobility is constant ; (4) substrate doping is uniform ; (5) reverse saturation current is very small ; (6) tranverse field is much larger than the longitudinal field (in y direction) ; (7) surface depletion charge is constant after inversion has occurred.

Total charge induced in the semiconductor per unit area Qs at a distance y from the source is given by

$$Q_s(y) = -[V_{GS} - \psi_s(y)].C_{ox}$$

where C_{ox} = gate oxide capacitance per unit area.

The charge in the inversion layer is given by

$$Q_n(y) = Q_s(y) - Q_B(y)$$

$$= -[V_{GS} - \psi_s(y)]\, C_{ox} - Q_B(y)$$

The surface potential $\psi_s'(y)$ at inversion can be approximated by $2\psi_B + V(y)$. The charge in the surface depletion region is given by

$$Q_B = - 2 \epsilon_o \epsilon_s q N_A(2\psi_B)$$

substituting this expression into the expression of $Q_n(y)$, yields

$$Q_n(y) = -[V_{GS}-V(y)-2\psi_B]\, C_{ox} + 2 \epsilon_o \epsilon_s q N_A(2\psi_B) \qquad (2.1)$$

The conductivity of the channel can be approximated by

$$\sigma(X) = q\, n(X)\, \mu_n(X)$$

where q = electronic charge, μ_n = electron mobility ;

n(X) = electron concentration in inversion layer.

The channel conductance is then given by

$$g = \frac{W}{L} \int_0^{X_i} \sigma(X)\, dX$$

for constant mobility case

$$g = \frac{W}{L}\, \mu_n\, |Q_n|$$

Channel resistance of an elemental section of length dy is given by

$$dR = \frac{dy}{L} = \frac{dy}{W\, \mu_n |Q_n(y)|}$$

The voltage drop across this section is

$$dV = I_{DS} \cdot dR = \frac{I_{DS}\, dy}{W\, \mu_n |Q_n(y)|} \qquad (2.2)$$

Substituting eqn. (2.1) into eqn. (2.2) and integrating from source (y = 0, V = 0) to drain (y = L, V = V_{DS})

$$dV = \frac{I_{DS}\, dy}{W\mu_n[(V_{GS}-V(y)-2\psi_B)\, C_{ox} - 2\epsilon_o \epsilon_s\, q\, N_A(2\psi_B)]}$$

$$I_{DS} = \frac{C_{ox}}{L} W\, \mu_n \left[(V_{GS}-2\psi_B - \frac{2\epsilon_o \epsilon_s\, q\, N_A(2\psi_B)}{C_{ox}} - \frac{V_{DS}}{2})\, V_{DS}\right]$$

$$I_{DS} = \frac{C_{ox} W \mu_n}{L} [(V_{GS}-V_T) V_{DS} - \frac{V_{DS}^2}{2}]$$

$$= \beta[(V_{GS}-V_T)V_{DS} - \frac{V_{DS}^2}{2}]$$

where $V_T = 2\psi_B + \frac{2 \epsilon_o \epsilon_s q N_A (2\psi_B)}{C_{ox}}$

$\beta = \mu_n C_{ox} \frac{W}{L}$ also called gain of the transistor

At the onset of pinch-off (saturation) inversion layer charge at drain end is zero.

i.e., at $y(L) = V_{DSSAT}$, $Q_n(L) = 0$

$$Q_n(L) = 0 = C_{ox}(V_G-V_T-V_{DSSAT})$$

Therefore, $V_{DSSAT} = (V_{GS}-V_T)$

after pinch-off drain current essentially remains constant and it is given by

$$I_{DSSAT} = \frac{C_{ox} W \mu_n}{L} \frac{(V_{GS}-V_T)^2}{2} = \frac{\beta}{2} (V_G - V_T)^2$$

main effect of metal-semiconductor work function difference ϕ_{MS} and fixed oxide charge is to shift the threshold voltage, V_T, and it is given by

$$V_T = (\phi_{ms} - \frac{Q_f}{C_{ox}}) + 2\psi_B + - \frac{Q_B}{C_{ox}} .$$

where Q_f is the total fixed charges at the interface.

2.1.3 Effect of Temperature [5]

β and V_T have strong temperature dependence, β shows a 3/2 power relation because of mobility term in the expression

$$\beta^* = \beta(\frac{T}{T_o})^{-3/2}$$

where T_o is room-temperature and T is temperature in question. Temperature appears explicitly in the value of junction potential, ϕ and its temperature dependence is determined by

$$\phi(T) = \frac{KT}{q} \ln \frac{N_A N_D}{n_i(T)^2}$$

where n_i is intrinsic concentration and is given by

$$n_i(T) = 1.5E33 \times T^3 \times Exp(-E_{go}/KT)$$

Temperature dependence of bandgap energy E_g is given by

$$E_g(T) = 1.17 - \frac{4.73 \times 10^{-4} T^2}{(T+636)}$$

Q_f is approximately independent of temperature. Junction leakage current doubles in magnitude for each decade rise in temperature above room temperature. Higher order effects on the device performance and hence on circuit performance is discussed in the next section.

2.2 MOSFET MODEL INCLUDING HIGHER ORDER EFFECTS

In this section we will develop a set of simple equations to describe electrical characteristic of NMOS device. Later these equations will be used in the computer program.

The I_{DS}-V_{DS} behaviour of an NMOS device can be described satisfactorily by following set of simple equations for first order calculation purpose.

For NMOS non-saturation (linear) region of operation is defined when $V_{DS} < (V_{GS} - V_T)$ and drain current in this region is given by

$$I_{DS} = \beta[(V_{GS}-V_T)V_{DS} - \frac{V_{DS}^2}{2}] \qquad (2.3)$$

and saturation region of operation is defined as $V_{DS} \geq (V_{GS} - V_T)$ and drain current is given by

$$I_{DS} = \frac{\beta}{2} (V_{GS} - V_T)^2 \qquad (2.4)$$

Equations (2.3) and (2.4) define the characteristic of the NMOS device.

A higher level model of MOSFET will include drain effect, mobility variation due to cross field and saturation of carrier velocity, channel length modulation and body bias effect on the device performance. To characterize accurately a scaled-MOSFET, inclusion of such effects is necessary. It is possible to obtain a set of equations in terms of process and physical

parameters of the device, which can accurately model all such higher order effects. Such a model will become very complex and may not be suitable for the use in circuit simulation where large number of devices will be used. Therefore, our objective is to construct a mathematical model with modified equations, which can be conveniently used to obtain sufficiently accurate results. We shall now briefly discuss the various higher order effects and the necessary modifications in the basic equations, to take these effects into account.

2.2.1 Drain Effect [5,6,8,9]

Drain potential affects the drain current in two ways.

(I) V_T reduces with increasing drain-substrate reverse bias; as the drain voltage increases the drain-substrate junction depletion region extends in the region below the gate. This effectively reduces the amount of charge to be contributed by the gate to form a conductive channel from source to drain. As a result, lesser amount of voltage at the gate node is required to invert the semiconductor type below the gate.

(II) β of the device increases with increasing drain voltage; as the drain depletion region extends in the channel, the effective length of channel also reduces by the same amount. This effect is more dominating in saturation region and give rise to finite conductance in this region.

This effect can be modelled by multiplying the drain current equation by an empirical relation as follows :

$$I_{DS} = I_{DS}(1 + \lambda V_{DS})$$

where λ = a constant 0.02 to 0.08 .

2.2.2 Body Bias Effect [9] :

Threshold voltage increases with increasing reverse bias between source and substrate. The body bias reduces the depletion region charge by an amount ∇Q_D and hence threshold voltage goes up by $\nabla V_T = - \nabla Q_D / C_{ox}$. Including the junction potential, the expression of threshold voltage is given by

$$V_T^* = V_T + \gamma[(2\psi_B - V_{BS})^{1/2} - (2\psi_B)^{1/2}]$$

where $\gamma = 2 \epsilon_o \epsilon_s q N_A)^{1/2} / C_{ox}$

Normally γ lies within 0.3 to 0.7 .

This expression needs modification for channel lengths less than 7.5 microns.

2.2.3 Mobility Variation [7] :

Due to presence of cross electric field and interface states and surface defects, surface mobility reduces. Mobility term appear in the expression of gain. Crawford [7] suggested the following empirical relation to take this effect into account,

$$\mu^* = \frac{\mu_o}{1 + \Theta(V_G - V_T^*)}$$

where Θ = a factor generally lies within 0.015 to 0.08 V^{-1}.

The complete set of modified equations is given below

Non-saturation case : $V_{DS} < V_{GS} - V_T^*$

$$I_{DS} = \beta^* \left[(V_{GS}-V_T^*) V_{DS} - \frac{V_{DS}^2}{2}\right] \qquad (2.5)$$

saturation case : $V_{DS} \geq V_{GS} - V_T^*$

$$I_{DS} = \frac{\beta^*}{2} [V_{GS} - V_T^*]^2 \cdot [1 + \lambda V_{DS}] \qquad (2.6)$$

where

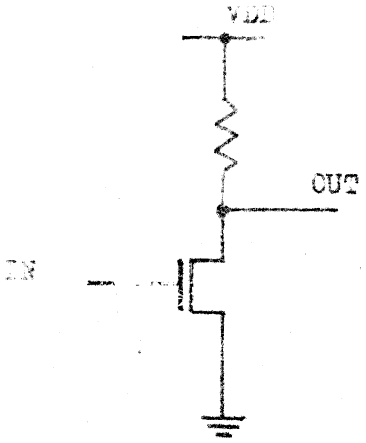
$$V_T^* = V_{TO} + \gamma[(2\psi_B - V_{BS})^{1/2} - (2\psi_B)^{1/2}]$$

2.3 BASIC MOS LOGIC CIRCUITS

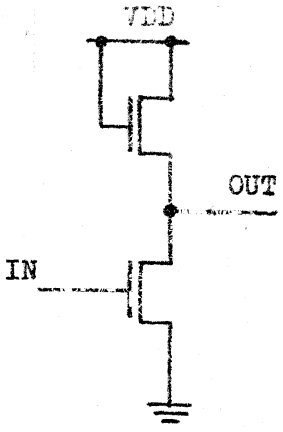
The first logic circuit we will describe is the inverter. It performs the logic operation of negation. The concepts developed in the analysis of inverter circuit will be extended further to NOR and NAND gates.

2.3.1 Inverter [2,9,10]

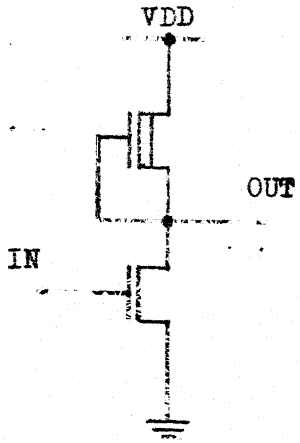
A simple inverter scheme is to use resistive pull-up and enhancement device pull-down as shown in Figure 2.3. When input is logical 1 (approximately equal to V_{DD}) and it is larger than threshold voltage q the enhancement pull-down



(a) RESISTIVE PULL-UP



(b) ENHANCEMENT PULL-UP



(c) DEPLETION PULL-UP

FIG. 2.3 INVERTERS

device then the pull down transistor will switch on and output. Voltage will start decreasing. To pull-down the output voltage below the threshold voltage of the device, it is required to have a sufficiently high load resistance. Thus to produce a compatible voltage level of logic 0, a high load resistance is needed. Similarly when input is logical zero (voltage level smaller than V_T) then output voltage will tend to rise upto V_{DD}. For a fast rising to V_{DD} it requires that load resistance should be as small as possible. Therefore, we see that load resistance should have a nonlinear nature to offer minimum resistance to the high going output and offer maximum resistance to the low going output. A load resistance having these properties can be obtained by depletion type transistor. With depletion type transistor as a load, $V_{out}(1)$ will go upto V_{DD} and V_{out} (0) will go well below V_T. The transient performance is also improved.

Another alternative of load transistor is to use an enhancement device connected to operate in saturation region. But it is observed that inverters using saturated enhancement load transistor are poor in transient performance. Other serious drawback of such circuit is that output voltage corresponding to logic 1 can never go to V_{DD}, it will always be less than $(V_{DD}-V_T)$ i.e., logic-swing has reduced. This reduces the drive or subsequent inverter. The enhancement load device can also be used in the linear region but it requires two power supplies.

2.3.2 Choice of W/L Ratio

For static characteristic calculation, currents through the load can be directly equated to current being sinked by driver transistor. Inter-stage d.c. current flow is zero because of high input impedance.

Let us assume that $V_{DD} = 5V$

$V_{IN} = V_{DD}$

$V_{TE} = 0.2\ V_{DD}$: Threshold voltage of enh. device

$V_{TD} = -0.8\ V_{DD}$: Threshold voltage of dep. device

When input to the inverter is at logic '1', output produces a logic '0'. In order to produce a compatible logic '0', it is necessary that voltage $V_O(0)$ should be smaller than V_{TE}. This can be further ensured by allowing a NM_0 (Noise-margin when output is high) of 0.5 Volts.

Assuming load is in saturation and the driver is in non-saturation.

$$I_{load} = \frac{\beta_L}{2} V_{TD}^2 \qquad (2.7)$$

$$I_{driver} = \beta_D[(V_{IN}-V_{TE})V_O(0) - \frac{V_O^2(0)}{2}] \qquad (2.8)$$

equating equations (2.7) and (2.8) and writing $B_R = B_D/B_L$

$$B_R = \frac{(V_{TD})^2}{2(V_{IN}-V_{TE})\ V_O(0)-V_O^2(0)}$$

substituting the various parameters we get

$$\beta_R = 4 : 1$$

Absolute values W/L for load and driver device is determined by the specification of power dissipation and speed. This has been illustrated with a detailed example in the next chapter. Inverters being driven by pass transistor experience a reduced drive at the input which will affect the logic (0) voltage level at the output. Therefore, β_R of such stage driven by pass transistor is generally increased to 8:1. Noise-margin is the measure of immunity of the circuit to the voltage spikes and device parameter variation. Logic threshold is that input voltage when output voltage is equal to input voltage but swing tendency is opposite to that of input. Usually $V_{T_{Logic}} = 0.5\ V_{DD}$.

2.3.3 Delays [2,9]

In a practical circuits minimum requirement of an inverter is that to drive another inverter, identical to itself. Therefore, it is necessary to analyse the performance of an inverter connected in the circuit and which is driving another identical inverter. Example of such circuit is an inverter chain (delay line) formed by cascading the identical inverters as shown in Figure 2.4. Each inverter is having 1 fan-in and 1 fan-out. β_R of the inverter is chosen to obtain proper logic levels.

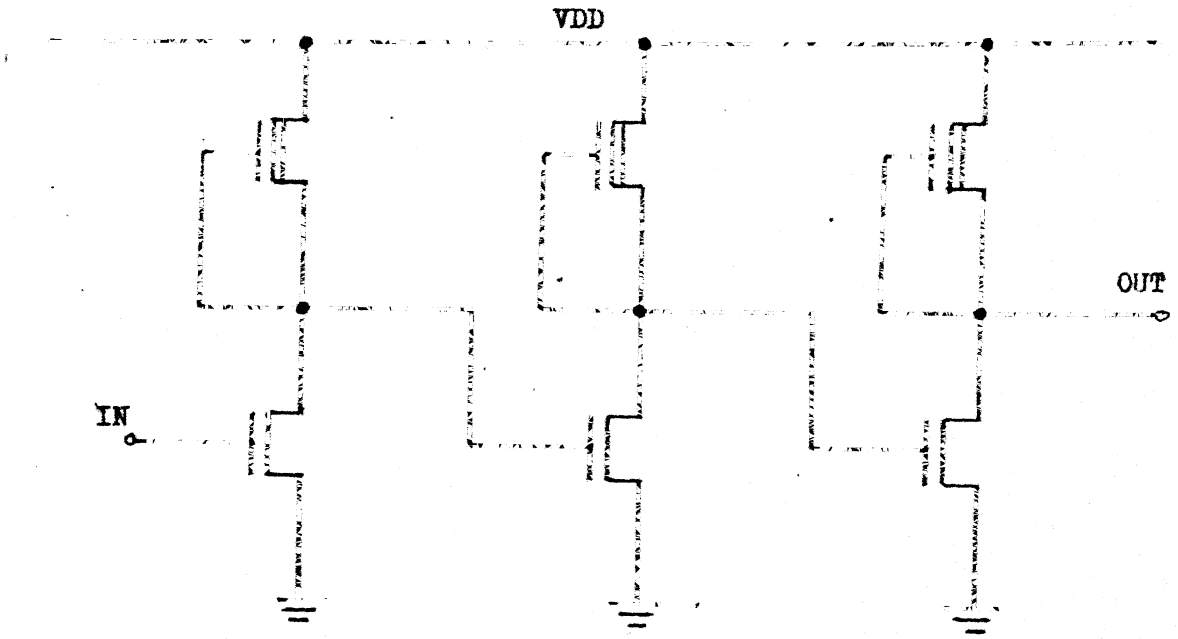


FIG. 2.4 INVERTER PAIR

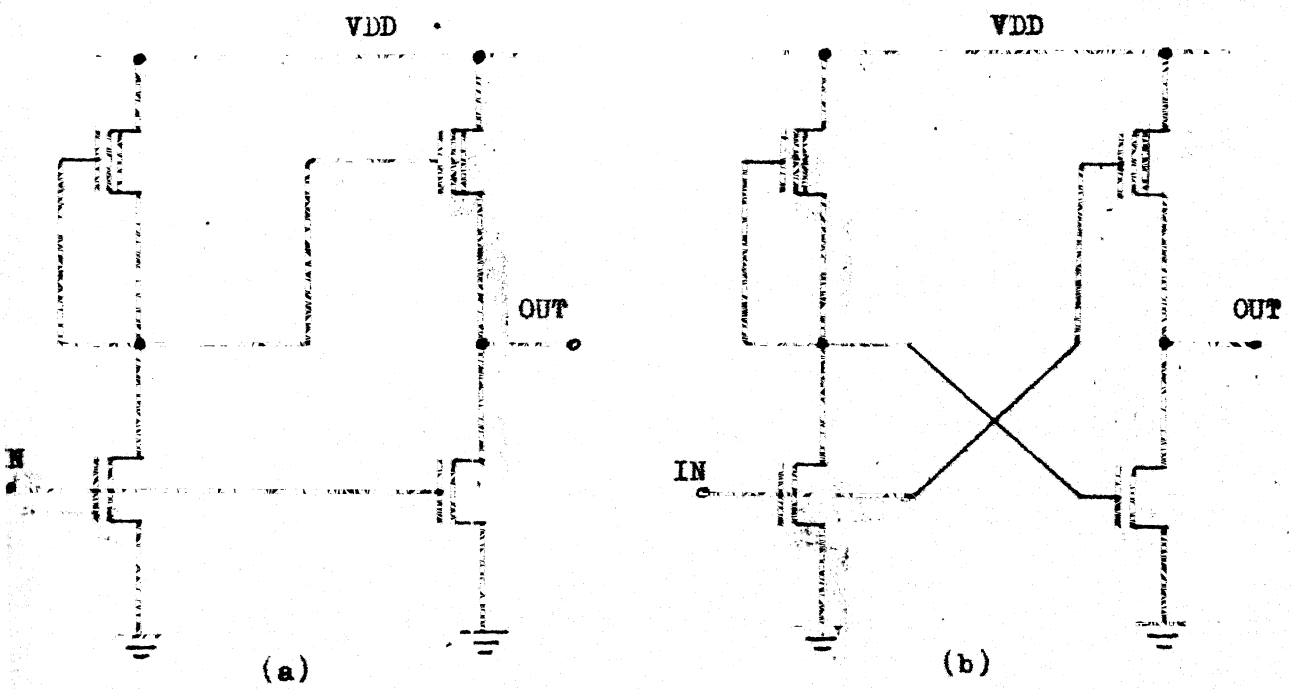


FIG. 2.5 SUPER BUFFER (a) INVERTING
(b) NON-INVERTING

levels. We shall now discuss about the overall delay of such a circuit.

Initially the circuit is in steady-state with O input at the first inverter. At t = O, input to first inverter changes to 1 (V_{DD}). Within approximately one transit time τ, (time taken by the carriers to cross the channel, given by $L^2/\mu.V_{DS}$), the pull-down of the first inverter will discharge the output node by removing the charge equal to V_{DD} times the gate capacitance of the pull-down transistor of the second inverter. Now, pull-down transistor of second inverter is off and hence its pull-up transistor has to supply a similar charge equal to V_{DD} times gate capacitance to the gate of pull-down transistor of the next (third) inverter. Since it can supply only $1/\beta_R$ of the current that can be supplied by pull-down transistor, the delay in the second stage is approximately β_R times that of the first.

We define inverter pair delay as sum of times taken by one high going and one low going transitions. In case of fan-out, f, the inverter pair delay increases by a factor equal to f.

To estimate the delay introduced by the single inverter driving a capacitive load, following assumptions are made.

1. There is no inherent delay of the device.
2. During charging of the output node, current is supplied, only by load device and driver is completely off. Similarly during discharging of the output node, current contribution from load device is zero.

T_{on} and T_{off} are fall time and rise time respectively within the limits of 0.1 V_{DD} and 0.9 V_{DD}.

T_{off} can be further divided into two parts t_1 and t_2 during t_1 load device operates in saturation and during t_2, it operates in nonsaturation.

(a) time t_1 : Equating the current of saturated load device to current flowing into the capacitor load.

$$C_L \frac{dv}{dt} = \frac{\beta_L (V_{TD})^2}{2}$$

where C_L = load capacitance, V_{TD} = threshold voltage of load device.

integrating with proper limits results,

$$t_1 = \frac{2\, C_L}{\beta_L} \frac{(V_{DD}+V_{TD})}{V_{TD}^2}$$

(b) time t_2 : Equating the capacitor current to the current supplied by load (operating in triode region),

$$C_L \frac{dv}{dt} = \beta_L \left[(-V_{TD})(V_{DD}-v) - \frac{1}{2} (V_{DD}-v)^2\right]$$

integrating from $(V_{DD}+V_{TD})$ to $0.9\ V_{DD}$ we obtain

$$t_2 = \frac{C_L}{\beta_L V_{TD}} \ln \left[\frac{0.1\ V_{DD}}{-0.1\ V_{DD}-2V_{TD}} \right]$$

Total rise time is $T_{off} = t_1+t_2$

$$T_{off} = \frac{C_L}{\beta_L V_{TD}} \left[\frac{2(V_{DD}+V_{TD})}{V_{TD}} + \ln\left(\frac{0.1\ V_{DD}}{-0.1\ V_{DD} - 2\ V_{TD}} \right) \right]$$

If $V_{TD} = -0.8\ V_{DD}$

then $T_{off} = T_{rise\ time} = \frac{4\ C_L}{\beta_L\ V_{DD}}$

Similarly for

$$T_{on} = T_{fall\ time} = \frac{4\ C_L}{\beta_D\ V_{DD}}$$

It can be shown that rise time to fall time ratio is equal to β_R, i.e.,

$$\frac{T_{off}}{T_{on}} = \frac{\beta_D}{\beta_L} = \beta_R \ .$$

2.3.4 Delay Minimization [2]

When a large capacitive load is driven by simple inverter, it causes a serious delay. Driving PLA inputs, control lines in memory cell, driving the off chip wires often present such situation. In such cases an optimum way to drive the load is to use cascaded elementary stages of inverter of increasing geometry until at some point that large capacitance can be directly driven by the stage using a large geometry inverters.

It can be shown that the total delay will be minimum if the ratio of size of a inverter stage to that of previous stage is e, the base of natural logarithm.

$$\text{Total minimum delay } t_{min} = \tau . e . \ln \left(\frac{C_L}{C_g}\right) .$$

2.3.5 Super Buffer [2,9]

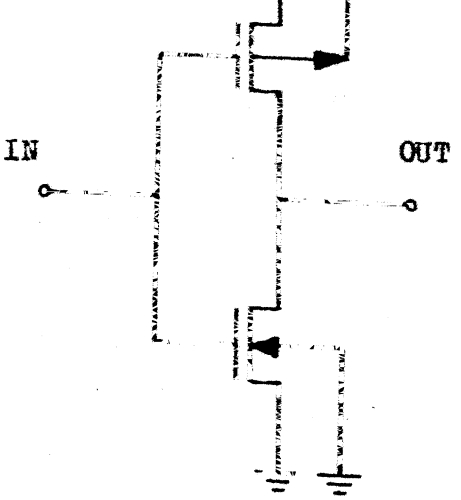
All ratio type inverters suffer from asymmetrical rise time and fall time in the output waveforms while driving capacitive load. This asymmetry is due to unequal current sourcing and sinking capability of load and driver respectively. To avoid this asymmetry we generally use super buffers as drivers which offers approximately symmetrical capability of current sourcing and sinking into a capacitive load. Inverting and noninverting circuits are shown in Fig. 2.5. Both uses depletion pull-ups with a ratio of β_R = 4:1, as in the standard inverters. In case of inverting buffer output of the first inverter drives the gater the pull-up of the second stage while the pull-down of the second stage is directly connected to the input. When input become zero the gate of pull-up rapidly reaches V_{DD} since it is the only load for the first inverter, and the depletion type load of the second inverter will turn on with approximately twice the drive it would experience if it's gate were tied to its source. Since the current from a device in saturation goes approximately square of the gate voltage, the current sourcing capability

of the supper buffer inverter is approximately four times that of a standard inverter. Hence, super buffers are invariably used to drive large capacitive loads, for example, I/O buffers of PLA, control and address lines in memory structures etc. Super buffer can also be used in cascaded inverter fashion as described earlier.

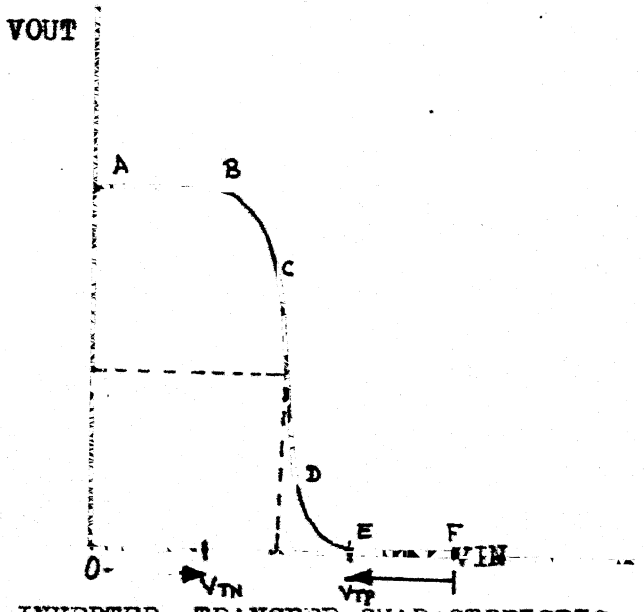
2.3.6 The CMOS Inverter [9,11,13]

The use or P-channel MOSFET as a load for an N-channel MOSFET driver provides the basic CMOS inverter circuit schematic as a CMOS inverter is shown in Fig. 2.6a. The driver is transistor Q_1, which is N-channel, and Q_2 act as load which is P-channel. The two MOSFETs are connected in series with the drains tied together and their gates having a common input, G. The drain point is the output of the inverter, CMOS circuits can be fabricated using P-well, N-well or twin-tub CMOS technologies.

The basic inverter operation can be explained as follows. Figure 2.6b presents the transfer characteristic of CMOS inverter. It is assumed that $|V_{TN}|+|V_{TP}| < V_{DD}$, which is a normal condition. Assuming V in is increasing from '0' to V_{DD}. In region A-B, Q_1 is off and Q_2 is operating in nonlinear region near the origin of its output characteristic. At C, Q_2 is at the verge of saturation where $V_O - V_{DD} = V_{in} - V_{DD} - V_{TP}$ yielding $V_O = V_{in} - V_{TP}$. Also Q_1



(a) CMOS CIRCUIT SCHEMATIC



(b) CMOS INVERTER TRANSFER CHARACTERISTIC

FIG 2.6 CMOS INVERTER

is operating in saturation and it tends to be less saturated. During C-D both load and driver are operating in saturation and a d.c. current is drawn from the supply, At point D, driver Q_1 is at the verge of saturation where $V_O = V_{in} - V_{TN}$. Between D and E, Q_1 is unsaturated and Q_2 is saturated. If input voltage V_{in} increase further, causes Q_2 to turn off and the only conducting transistor Q_1 pulls down the output near ground. CMOS gate offers many advantages, including high noise immunity, operation at a wide range or power supply voltages, low power dissipation relatively high speed, and compatibility to other gates. The only disadvantage is that it requires relatively larger chip area. Transient characteristic of CMOS inverter is explained below.

(1) When V_{in} = logic (O)

i.e. $V_{in} = V(O)$, $V(O) < V_{TN}$

then driver is off, where V_{TN} is the threshold voltages of N-channel device.

If $|(V(O)-V_{DD})| > |V_{TP}|$

where V_{TP} is the threshold voltage of P-channel device. then load is on.

T_{off}, charging time is given by

$$T_{off} = T_p \left[\frac{2}{\frac{V_{DD}}{|V_{TP}|} - 1} + \ln \left(\frac{2(V_{DD}-|V_{TP}|)}{V_{DD}-V(1)} - 1 \right) \right]$$

where $T_p = \frac{C_{out}}{\beta_L(V_{DD}-|V_{TP}|)}$

(2) When V_{in} = logic 1

i.e., $V_{in} = V(1), \quad V(1) > V_{TN}$

then driver is on

If $|V(1) - V_{DD}| < |V_{TP}|$

then load is off

T_{on}, discharge time is given by

$$T_{on} = T_n \left[\frac{2}{\frac{V_{DD}}{V_{TN}} - 1} + \ln\left(\frac{2(V_{DD}-V_{TN})}{V(O)} - 1\right)\right]$$

where

$$T_n = \frac{C_{out}}{\beta_D(V_{DD}-V_{TN})}$$

Logic threshold of CMOS gate is close to $\frac{V_{DD}}{2}$ if symmetrical devices are used, i.e., $\beta_D = \beta_L$. The $\beta_D = \beta_L$ condition can be achieved if $[(\frac{W}{L})_{PMOS}/(\frac{W}{L})_{NMOS}] = \frac{\mu_n}{\mu_p} = 2.5$.

CMOS inverter delay T_D is designed as time delay between input and output waveforms at $V_{DD}/2$ points.

$$T_D = \frac{0.9\ C_{out}}{V_{DD}\ \beta_D}\left[\frac{1}{(1 - \frac{V_{TN}}{V_{DD}})^2} + \frac{1}{\frac{\beta_L}{\beta_D}(1 - \frac{|V_{TP}|}{V_{DD}})^2}\right]$$

If $(V_{TN}/V_{DD}) \ll 1$ and $\frac{|V_{TP}|}{V_{DD}} \ll 1$ then

$$T_D = \frac{0.9\ C_{out}}{V_{DD}\ \beta_D}\left[1 + \frac{\beta_D}{\beta_L}\right]$$

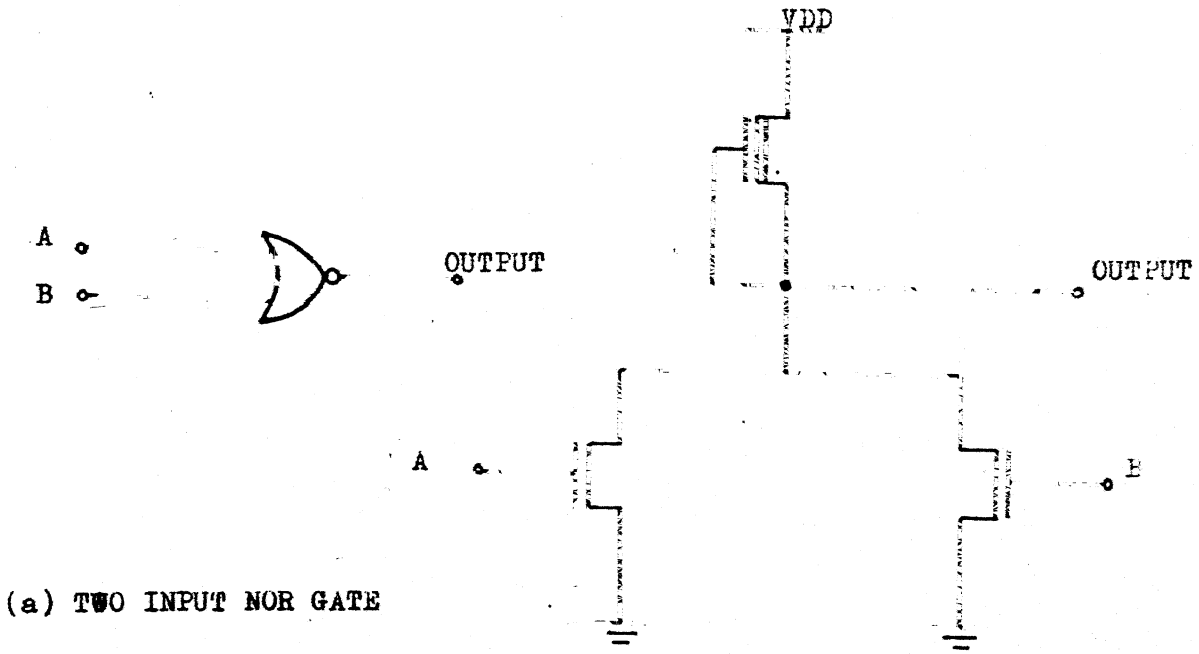
In these conditions V_{TN} and V_{TP} have a small effect over the delay time and T_D is largely proportional to (C_{out}/V_{DD}) and β_D^{-1}. It is clear that minimum value of V_{DD} is $V_{DD}|_{min} = V_{TN} + |V_{TP}|$. If V_{DD} is lower than that value, the gate demonstrates a hysteresis transfer curve.

2.3.7 NOR Gate

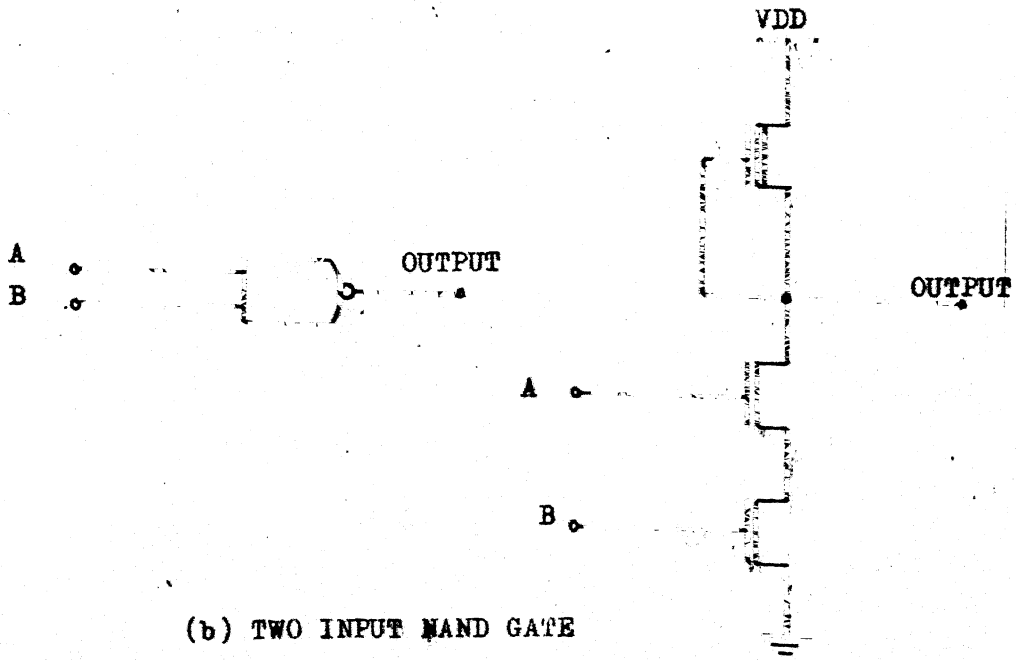
The circuit diagram of 2-input NOR gate is shown in Fig. 2.7a. Basically it is an inverter with additional enhancement mode transistors in parallel with the pull-down of the inverter. Additional inputs can be added in the same way. If either of the two inputs is 1, the pull-down transistor will switch on and output will be driven low. For both inputs zero, both the pull-downs are off and output is driven high upto V_{DD}. Ratio W/L of each pull-down to that of common pull-up is generally kept 4:1. Therefore, if only one input is active (rest all are fixed at zero) then the logic threshold voltage and voltages of logic levels will be similar to that in standard inverter. However, when two or more inputs are high simultaneously then output voltage corresponding to logic 0, V(0) will be less than that in the standard inverter.

2.3.8 NAND Gate

This gate can also be constructed as simple extension of the basic inverter circuit. The analysis of the behaviour of these circuit is a direct extension of the analysis of the basic



(a) TWO INPUT NOR GATE



(b) TWO INPUT NAND GATE

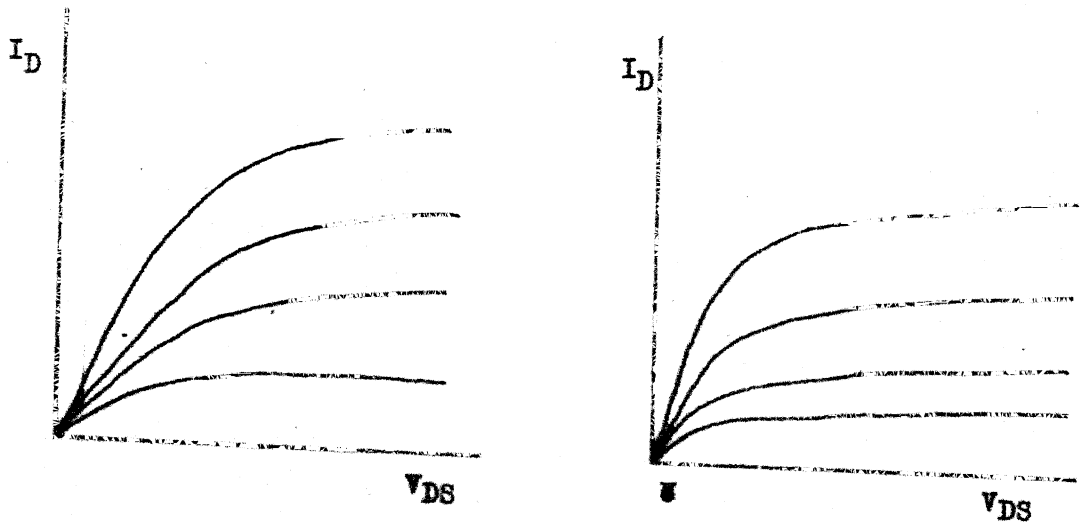
FIG. 2.7

inverter. Circuit diagram of NAND gate is shown in Fig. 2.7b. A 2-input NAND gate can be obtained by addition of an enhancement transistor in series with the driver of the inverter. For more inputs, more transistors can be added in the same manner. If either of input is '0' then the corresponding transistor will be off and output will remain at logic 1. When all the inputs to the NAND gate are logical 1, then output node will be pulled down to low voltage by the stack of drivers. As inputs are added, effective channel length of the pull down will be of the channel lengths of transistors in series. This may increase the logical threshold voltage greater than that of standard inverter. To circumvent this problem general approach is to increase the W/L ratio of the transistors connected in series by a factor, equal to number of transistors connected in series.

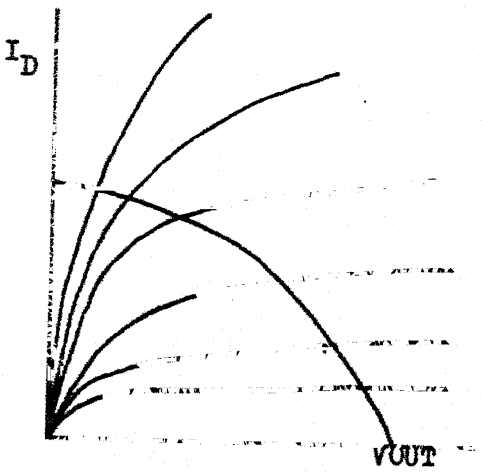
2.4 CIRCUIT SIMULATION

2.4.1 D.C. Analysis [2]

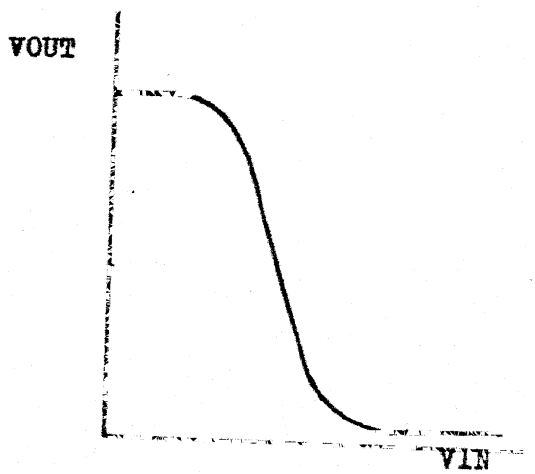
In this section we will present an algorithm for determination of actual transfer characteristic of the inverter. This is explained for graphical determination to illustrate the algorithm. This can be easily extended for computer simulation of any MOS circuits.



A (a) I - V CHARACTERISTICS



(b) I_D - VOUT PLOT



(c) TRANSFER CHARACTERISTICS

FIG. 2.8

From the figure 2.8, $(V_{DD} - V_{DS}(dep))$ is equal to $V_{DS}(enh)$ and it is also equal to V_{out}. At steady state is no current is drawn from the output, the currents of two devices will be equal. Since gate of the pull up transistor is tied to its source only one of its characteristic corresponding to $V_{GS} = 0$, is relevent for its representation. By superimposing plots of $I_{DS}(enh)$ versus $V_{DS}(enh)$ and the one plot of $I_{DS}(dep)$ versus $[V_{DD}-V_{DS}(enh)]$ since current in both the device is same therefore cross section of the characteristic represents the V_{out} versus $V_{GS}(enh)$. For the period input is less than the threshold voltage of the enhancement driver, it remains off and output remains at V_{DD}. It can be seen that for larger values of β_R, the transfer characteristic is more steeper, and β_R should be greater than unity for digital circuit to function properly.

2.4.2 Transient Analysis

D.C. characteristic alone is not sufficient to predict the rise time, fall time of node voltage. The approximate relations for the same derived in the section 2.3.3 are useful from qualitative point of view. Inclusion of higher effects in calculations requires more powerful technique. Hence it is necessary to have a transient analysis program. In this section, transient analysis algorithm, its implementation, block structure and general description of the program is given. Three circuits of Inverter, NOR and NAND have been analysed and their results are discussed at the end of this chapter.

2.4.3 Implementation [14,15,16]

A computer program is developed for transient analysis of MOS transistor circuits. This program uses device model developed in Section 2.2. Newton-Raphson algorithm, for solution of system of nonlinear equations, is used. For transient analysis fixed time step Backward Euler technique is used. Program is written in FORTRAN and it uses one IMSL library routine.

2.4.5 Simulation Algorithm [14,16]

We shall now briefly describe the simulation algorithm step by step.

S1 : Variables used are initialized and flags are set. Call TIMER to start counting the job time.

S2 : Input datas are read from the port specified in S1 and then stored in arrays and variables.

S3 : Input datas are rescanned and stored in the output file in appropriate format. Various parameters of models are also evaluated and stored for further use.

S4 : If current time is more than simulation maximum time limit then simulation is stopped and timer is called to estimate total run time of the job, else continue.

S5 : Input sources are processed according to their specification of initial delay, initial value, final value and pulse width with respect to current simulation time.

S6 : If it is a D.C. analysis to determine initial conditions then skip to S8.

S7 : If it is a first iteration at any time step, then, lumped capacitors are processed and value of current source in the discrete Newton-Raphson model of capacitor is updated, else continue.

S8 : MOS transistors are processed according to their type and mode of operation at a particular biasing condition. Admittance matrix and equivalent current source vector is updated.

S9 : Admittance matrix and equivalent current vector are modified; rows and columns pertaining to nodes which are also the nodes of input sources are deleted and matrix is ordered for solution.

S10 : System of linearized equations are solved and node voltage array is updated.

S11 : Node voltage vector is reordered and voltages are correctly assigned to corresponding nodes.

S12 : If convergence has not reached or number of iterations at any time step is less than 10, then go to step S6, else continue.

S13 : If current time is greater than TSTART then plot output node voltage, else continue.

S14 : TIME is advanced by TSTEP and iteration control flags are reset.

S15 : If current time is greater than TSTOP then call TIMER to estimate total job time and then stop the simulation, else continue.

S16 : If number of points already plotted exceeds maximum limit of 80 points then call TIMER to estimate total job time and then stop the simulation, else go to S5.

2.4.5 Main Program and Subroutines

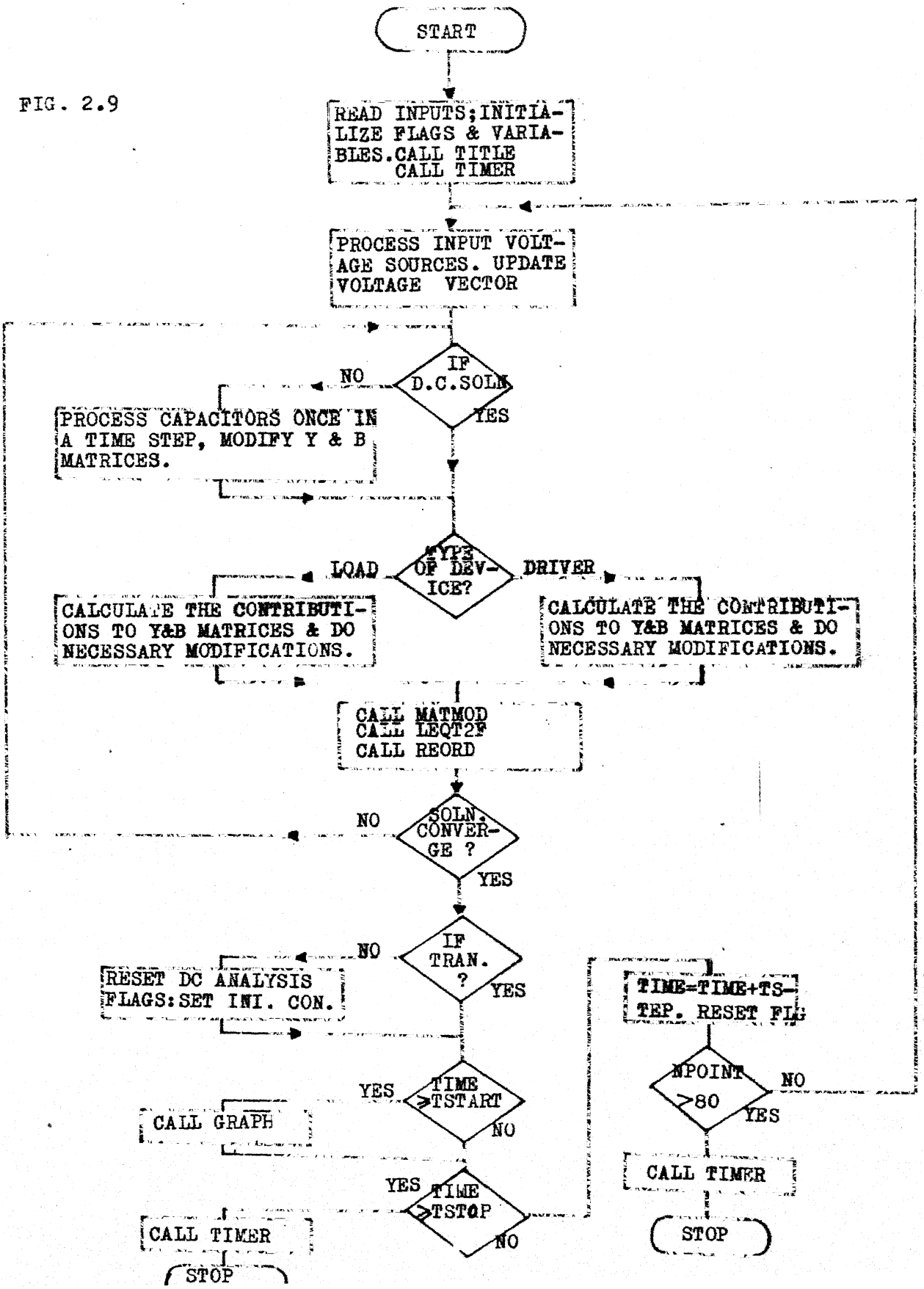
Main program is divided into many sections and it proceeds along the lines of simulation algorithm discussed in the previous section. Block diagram of the program is given in Fig. 2.9. Subroutines are used when necessary but otherwise sections are preferred in the main program. Flags are used in the program to control the flow of program. Variables TIME is current simulation time.

We shall now briefly describe the functions of different subroutines used in the program.

TITLE : It calculates the threshold voltage and other parameters of the MOSFET model and prints them in the output file. It also writes the title of the circuit as heading of each section in the output.

FLOW CHART FOR TRANSIENT ANALYSIS OF MOS CIRCUITS

FIG. 2.9



IDENTY: This subroutine identifies that a node is an external input node or an internal input node. It is necessary to avoid writing node equations at the node whose voltage is already known.

MATMOD : This subroutine modifies the node admittance matrix and equivalent current vector.

LEQT2F : This is a IMSL subroutine to solve the system of linear equations.

REORD : This is used to reorder the node voltage vector and assign voltages to corresponding nodes.

GRP : It is used for plotting the graph between output voltage and time.

SECOND : This macro is used as TIMER to calculate the total runtime for the program.

2.5 RESULTS AND DISCUSSIONS

The above program is used to analyse three basic configuration of MOSFETs which are very common in MOS circuits. The configurations are Inverters NOR and NAND gates. Input data are supplied in the format and order as described in Appendix Value of T_{ox} and N_{SUB} is adjusted to yield threshold voltage around 0.2 V_{DD} for enhancement and around -0.8 V_{DD} for depletion type device. Transient analysis output is plotted on graph against time. Loading condition is simulated by ing a load capacitor at the output node.

2.5.1 Inverter

A MOS E/D inverter as shown in Fig. 2.3.3 is analysed for transient behaviour. β_R is chosen to be 4:1. Output is shown in Fig. 2.10.

T_{rise} = 33 nano-seconds

T_{fall} = 11 nano-seconds

Logic level 1 = 5 volts

Logic level 0 = 0.6 volts

Average delay = 22 nano-seconds

2.5.2 NOR Gate

A two input NOR gate is realized in MOS circuit as shown in Fig. 2.7.a. W/L ratio of both the driver transistor is same and is equal to that of a driver in any standard inverter. When any one of the input goes high the output is driven to low value and when both of them are low then the output goes to V_{DD}. If both the inputs are high simultaneously then output goes further low than it would have gone if only one of the two inputs is on. This effect can be clearly observed in the output waveform shown in Fig. 2.11.

T_{rise} = 35 nano-seconds

T_{fall} = 12 nano-seconds

Logic Level 1 = 5 Volts

Logic Level 0 = 0.3 Volts

Average delay = 23.5 nano-seconds

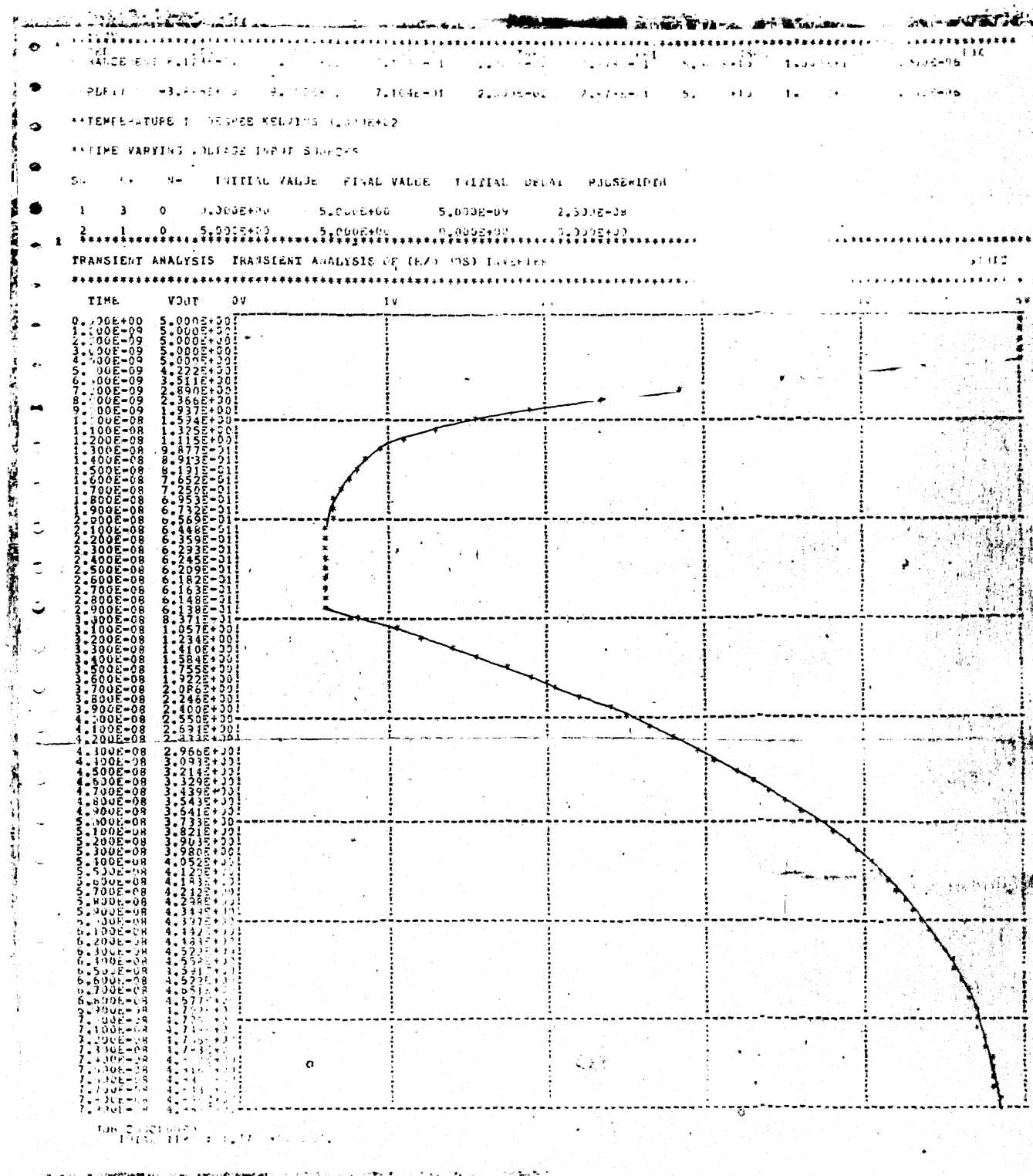


FIG. 2.10

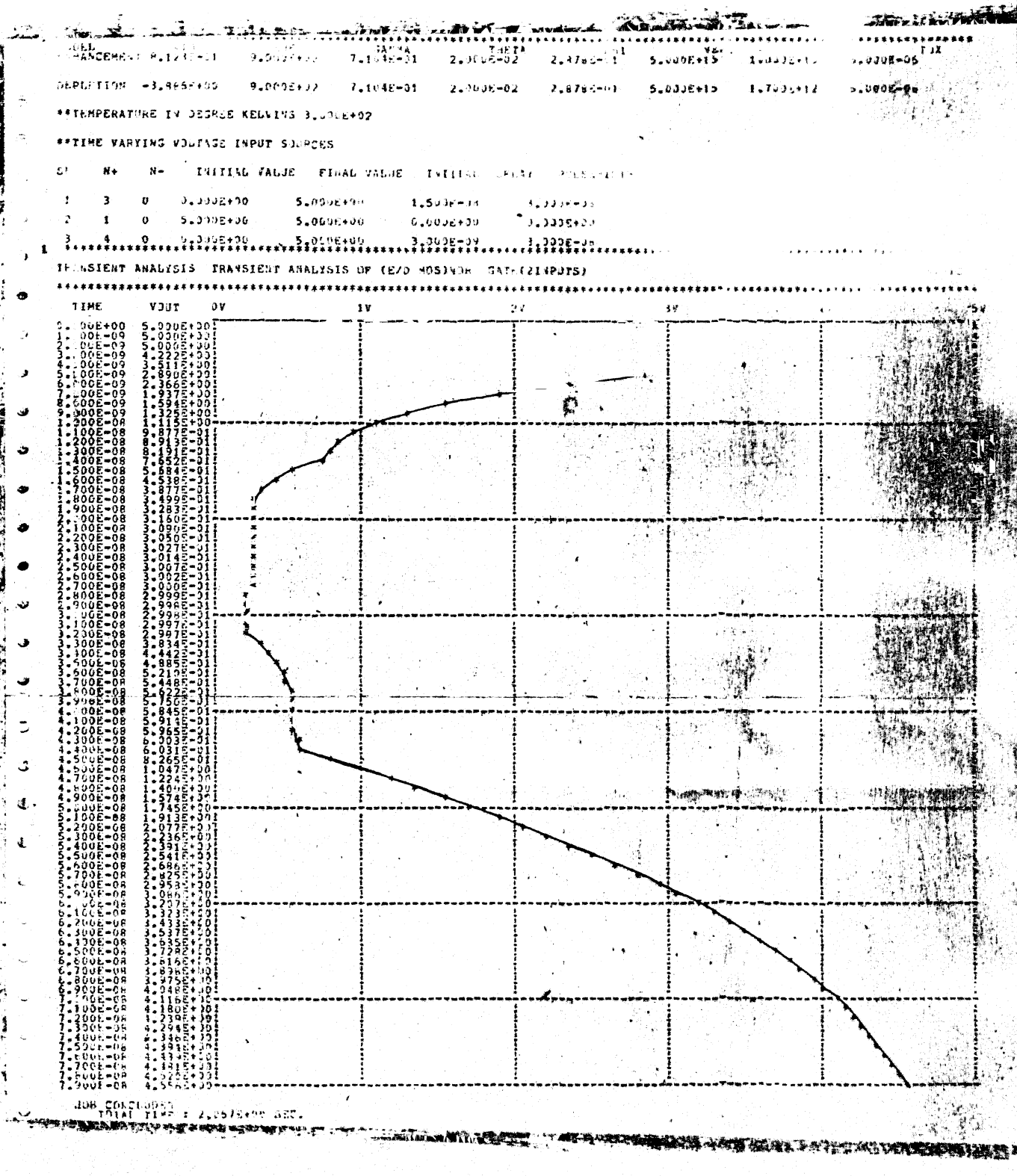

**TEMPERATURE IN DEGREE KELVINS 3.00E+02
**TIME VARYING VOLTAGE INPUT SOURCES
TRANSIENT ANALYSIS TRANSIENT ANALYSIS OF (E/D MOS)NOR GATE(2INPUTS)
TIME VOUT
0V
1V
2V
3V
5V
JOB CONCLUDED

FIG. 2.11

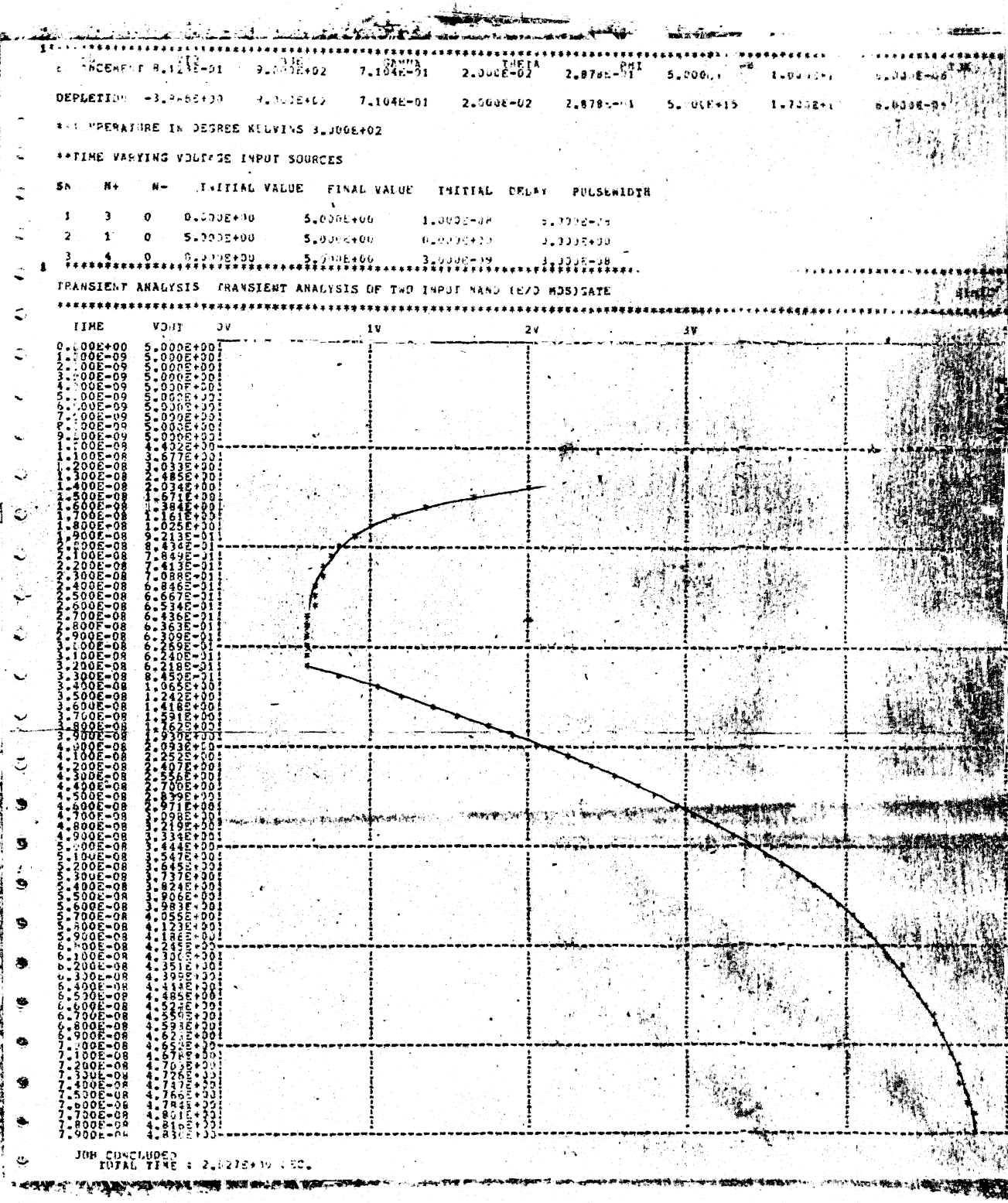

INCREMENT 8.125E-01 9.000E+02 7.104E-01 2.000E-02 2.878E-01 5.000E+
DEPLETION -3.968E+00 9.000E+02 7.104E-01 2.000E-02 2.878E-01 5.001E+15
TEMPERATURE IN DEGREE KELVINS 3.000E+02
**TIME VARYING VOLTAGE INPUT SOURCES
SN N+ N- INITIAL VALUE FINAL VALUE INITIAL DELAY PULSEWIDTH
1 3 0 0.000E+00 5.000E+00
2 1 0 5.000E+00 5.000E+00
3 4 0 0.000E+00 5.000E+00 3.000E-09
TRANSIENT ANALYSIS TRANSIENT ANALYSIS OF TWO INPUT NAND (E/D MOS)GATE
TIME VOUT
0.000E+00 5.000E+00
1.000E-09 5.000E+00
2.000E-09 5.000E+00
3.000E-09 5.000E+00
4.000E-09 5.000E+00
5.000E-09 5.000E+00
6.000E-09 5.000E+00
7.000E-09 5.000E+00
8.000E-09 5.000E+00
9.000E-09 5.000E+00
1.000E-08 4.402E+00
1.100E-08 3.677E+00
1.200E-08 3.033E+00
1.300E-08 2.485E+00
1.400E-08 2.034E+00
1.500E-08 1.671E+00
1.600E-08 1.384E+00
1.700E-08 1.161E+00
1.800E-08 1.025E+00
1.900E-08 9.213E-01
2.000E-08 8.436E-01
2.100E-08 7.849E-01
2.200E-08 7.413E-01
2.300E-08 7.088E-01
2.400E-08 6.846E-01
2.500E-08 6.667E-01
2.600E-08 6.534E-01
2.700E-08 6.436E-01
2.800E-08 6.363E-01
2.900E-08 6.309E-01
3.000E-08 6.269E-01
3.100E-08 6.240E-01
3.200E-08 6.218E-01
3.300E-08 8.459E-01
3.400E-08 1.065E+00
3.500E-08 1.242E+00
3.600E-08 1.416E+00
3.700E-08 1.591E+00
3.800E-08 1.762E+00
3.900E-08 1.939E+00
4.000E-08 2.093E+00
4.100E-08 2.252E+00
4.200E-08 2.407E+00
4.300E-08 2.556E+00
4.400E-08 2.700E+00
4.500E-08 2.839E+00
4.600E-08 2.971E+00
4.700E-08 3.098E+00
4.800E-08 3.219E+00
4.900E-08 3.334E+00
5.000E-08 3.444E+00
5.100E-08 3.547E+00
5.200E-08 3.645E+00
5.300E-08 3.737E+00
5.400E-08 3.824E+00
5.500E-08 3.906E+00
5.600E-08 3.983E+00
5.700E-08 4.055E+00
5.800E-08 4.123E+00
5.900E-08 4.186E+00
6.000E-08 4.245E+00
6.100E-08 4.300E+00
6.200E-08 4.351E+00
6.300E-08 4.399E+00
6.400E-08 4.443E+00
6.500E-08 4.485E+00
6.600E-08 4.524E+00
6.700E-08 4.559E+00
6.800E-08 4.593E+00
6.900E-08 4.624E+00
7.000E-08 4.653E+00
7.100E-08 4.679E+00
7.200E-08 4.703E+00
7.300E-08 4.726E+00
7.400E-08 4.747E+00
7.500E-08 4.766E+00
7.600E-08 4.784E+00
7.700E-08 4.801E+00
7.800E-08 4.816E+00
7.900E-08 4.830E+00
1V
2V
3V
JOB CONCLUDED
TOTAL TIME = 2.027E+00 SEC.

FIG. 2.12

2.5.3 NAND Gate

A two input NAND gate structure as shown in Fig. 2.7.b is analysed. W/L ratio of the two driver transistor is doubled (increased by a factor equal to number of transistors in series). When any of the input is low that transistor is off in the series combination, the output voltage remains high. When all the inputs are high then only output is driven low. If W/L ratio is not adjusted then the $V_{out}(O)$ may be higher than the threshold voltage of the driver device. Simulated output waveform is shown in Fig. 2.12.

T_{rise} = 33 nano-seconds

T_{fall} = 11 nano-seconds

Logic Level 1 = 5 volts

Logic Level O = 0.63 volts

Average delay = 22 nano-seconds

CHAPTER 3

MOS IC DESIGN METHODOLOGY

Logic circuits can be categorized in terms of combinational/sequential logic, static/dynamic logic. All these use similar circuit elements. For illustration, examples of EXOR, EXNOR. Flip-flop circuits have been worked out in great detail using nonstructured (Random)/structured approach of design. These circuits are then used as primitive building blocks in the realization of higher level functional blocks such as Full Adder, counter, etc.

Combinational logic forms the basis of all sequential logic design. An appropriate feedback with delay can change combinational circuit, to a sequential circuit. A dynamic shift register cell has been designed for illustration of design of dynamic logic. At the end some results of computer simulation of IC modules for electrical behaviour is given. Choice of proper parameters for accurate simulation is very necessary. Therefore, all parasitic capacitance/resistances have been estimated from the actual layout given at the end. Layout is prepared according to process and design rules as described by Mead and Conway [2].

3.1 LOGIC DESIGN WITH MOS [2,9,17]

A combinational logic circuit can be designed using any of

the following design methods :

(1) Random Logic : It is conventional form of arranging the transistors randomly to form the circuit, so as to obtain the desired input-output functional relationship.

(2) Structured Logic (PLA) : Programmable logic array is an efficient structured logic arrangement to design any arbitrary function. Overall structure of PLA remains same, the effect of arbitrary nature of function on design is limited to selectively placing the transistors in the array.

3.1.1 Stick Diagram [2]

Circuit diagram does not convey any idea about the layout of the circuit. Knowledge of layout is necessary to know the actual orientation and arrangement of transistors for compact realization and to find the solution of resulting complexity of inter-connect. For this, actual detailed layout will be very inconvenient and time consuming to make changes in the detailed layout. Stick diagram is the way to represent the layout by coloured sticks and special symbols. It is very convenient representation for use in CAD programs. Further, actual detailed layout can be obtained by expands the regions and lines to their dimension.

The colour codes used in the stick diagram are given below :

Red = Polysilicon ; Blue = Metal

Green = Diffusion ; Black= Contact-cuts

Yellow= ion-~~input~~ implant

crossing of green and red regions indicate presence of an enhancement transistor whose gate is controlled by signal on the red. If the crossing of red and green is overlapped with yellow region, it indicate a depletion type transistor. Following crossings of lines are allowed without any interference of the signals.

(1) Red and Blue lines

(2) Green and Blue lines.

Contact-cut just above the transistor is not allowed.However, a transistor can be formed below a metal line.

3.2 RANDOM LOGIC

In MOS technology, the basic building blocks are inverter, NOR and NAND gates. Apart from these gates, this technique offers the possibility of compact realization of functions using complex gates. A complex gate can be obtained by merging the structures of any two or more basic building blocks. Fig. 3.1.a shows the configuration of MOS transistors in inverter, NOR and NAND gates.

Logic level in terms of voltage of the node, depends upon W/L ratio of the transistors connected to that node. W/L ratio is also a factor in the expression of channel conductance.

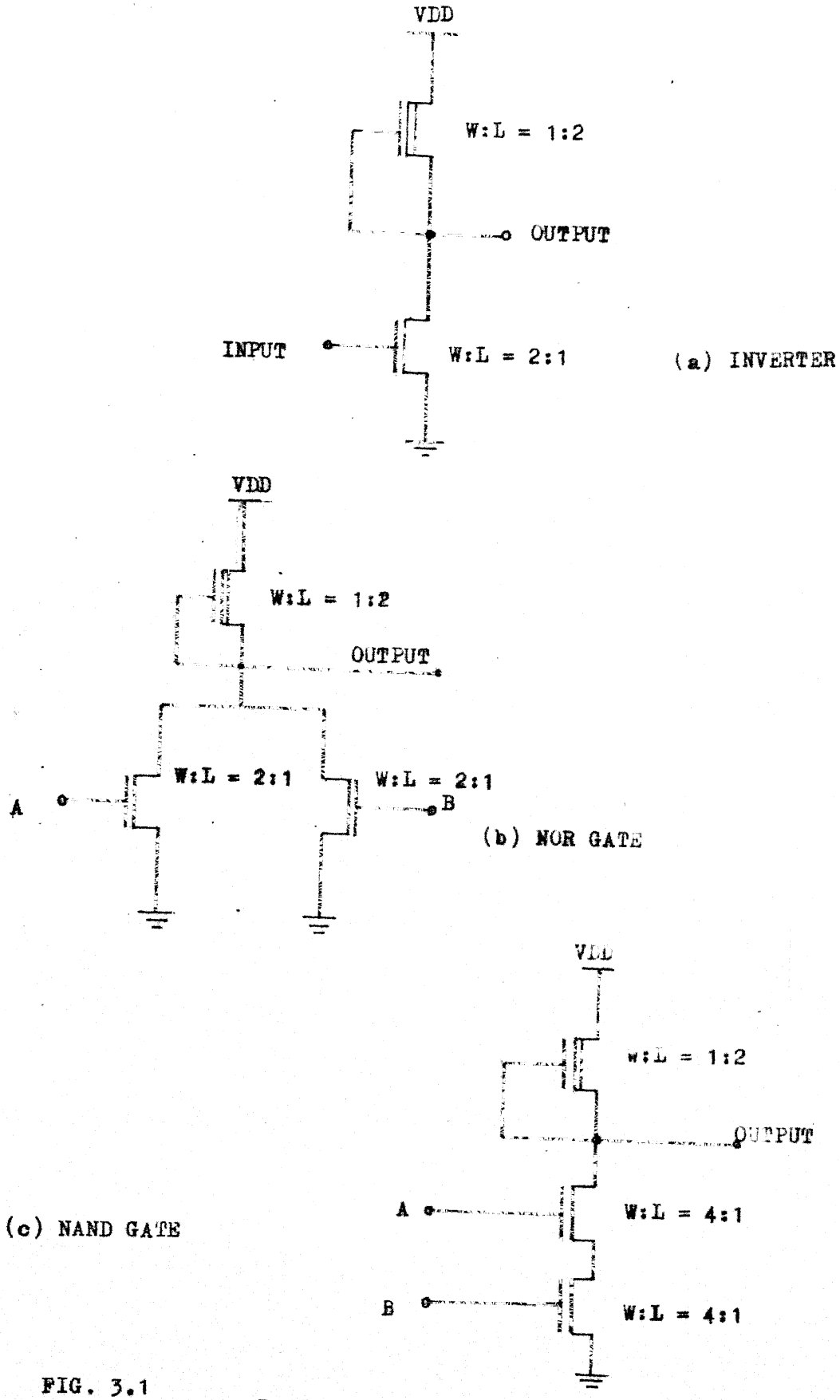


FIG. 3.1

BASIC BUILDING BLOCKS

In case of NOR circuit, when any one of the input goes high and other remains at zero, then the output node voltage representing zero logic output would be same as that of an standard inverter. But when both inputs go high simultaneously then output node voltage will further go down towards ground. This is shown in Fig. 3.1(b).

In case of NAND, input transistors are stacked. Therefore, when all the input transistors are ON, the total resistance between output node and ground is sum of ON resistances of the transistors. As a result the output node voltage will be N times that of standard inverter, where N is number of transistors in the stack. In order to make the output node voltage equal to that of standard inverter, W/L ratio of each transistor in stack, is increased by a factor of N. This is shown in Fig. 3.1(c).

Apart from Inverter, NOR and NAND gate structures, flip-flop and Exclusive-OR are also used extensively in MOS LSI as a building block. Generally, flip-flops are made by cross-coupled inverters. Exclusive-OR is constructed by a combination of complex gates and three basic gates. Therefore, with the idea of covering all by one example, design of EX-OR has been given in detail.

3.2.1 EXCLUSIVE OR

Exclusive-OR operation on two variable A and B is defined

as $A \oplus B = \bar{A}B + \bar{B}A$ where $\oplus$ is the notation to represent EX-OR operation. Logic realization of EX-OR function is not unique and so is the circuit design. In support of this statement, three different MOS circuits realizing the same function (EX-OR) is given in Fig. 3.2. Each of the circuit has a different approach and different number of device count. However, keeping in mind the optimal design, we can directly obtain circuit diagram. Layout for each of the three circuits has been obtained and on comparison it has been found that the circuit given in Fig. 3.2(c) offers minimum area of silicon chip. Therefore, design of only this circuit will be presented here.

Assuming $V_{DD} = 5$ Volts,

$V_{TE} = 0.2\ V_{DD}$ (Threshold voltage of enhancement type device),

$V_{TD} = -0.8\ V_{DD}$ (Threshold voltage of depletion type device)

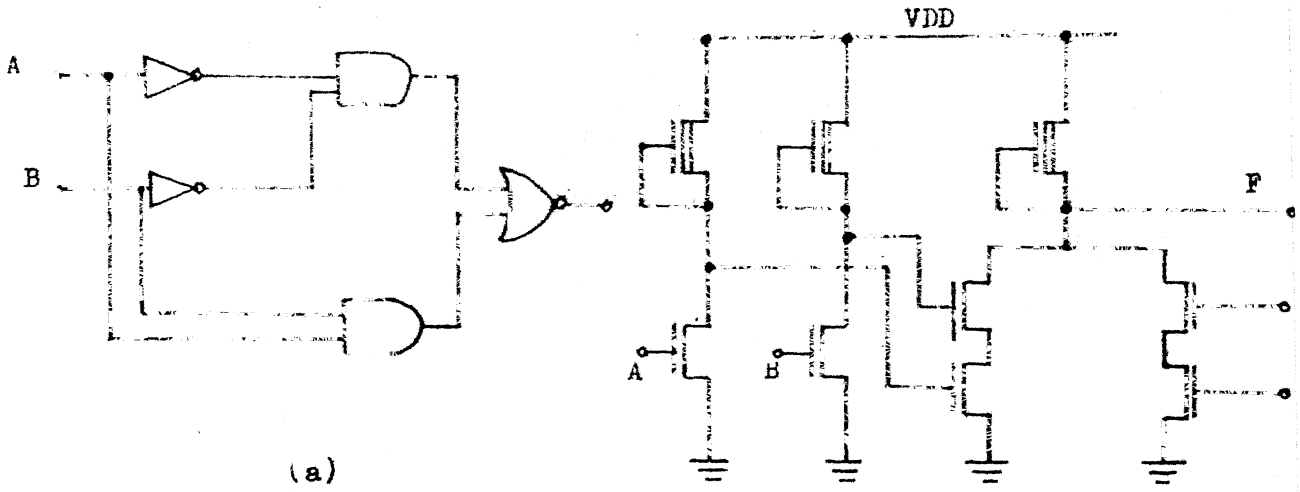
$NM^{o} = 0.5$ Volts

$V_{out(o)} = 0.5\ V_{TE}$

Output voltage depends upon W/L ratios and threshold voltages of driver and load transistors. The relationship is given as follows :

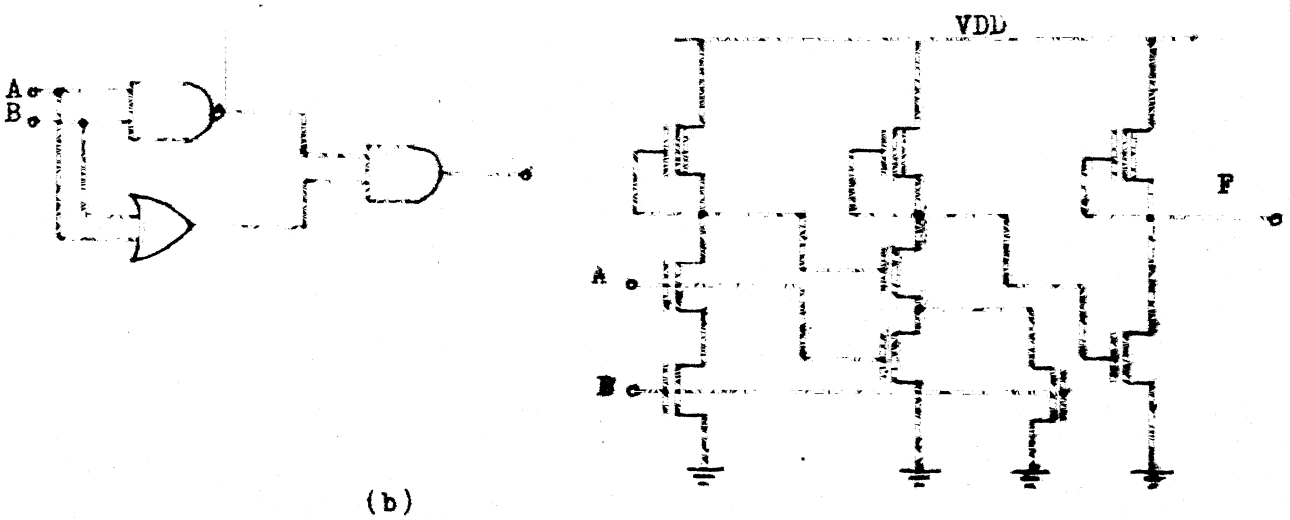
$$\beta_R = \frac{\beta_D}{\beta_L} = \frac{W/L_{Driver}}{W/L_{Load}} = \frac{(-V_{TD})^2}{2(V_{IN}-V_{TE})\ V_{out(o)} - V^2_{out(o)}}$$

substituting the values in the above equation we get

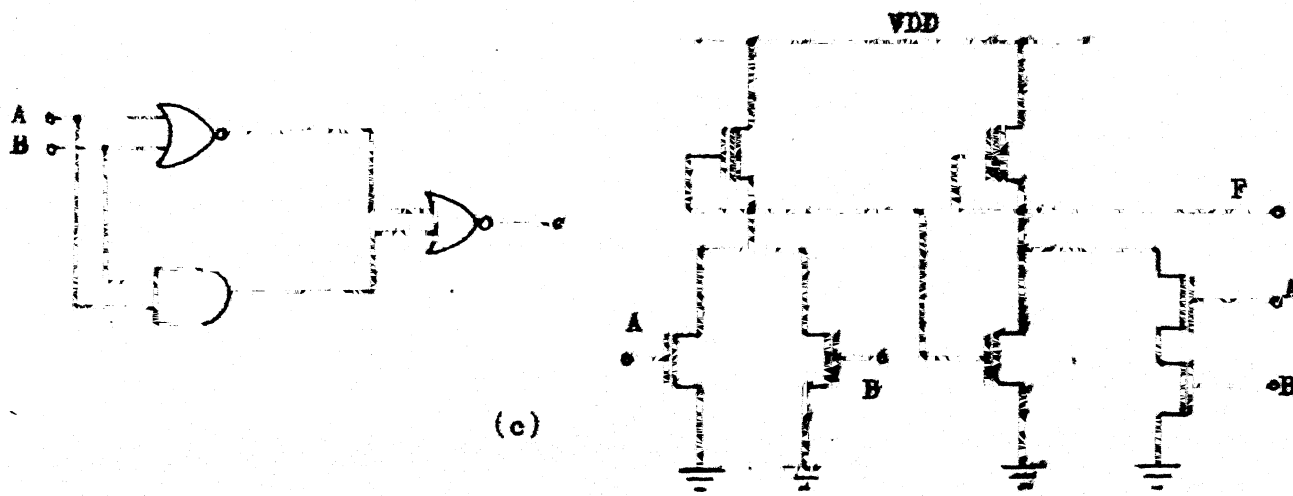


(a)

FIG. 3.2 EXCLUSIVE-OR CIRCUITS



(b)



(c)

$\beta_R = 4:1$

Choice of absolute values of W/L ratio of transistor (in standard inverter configuration) depends upon specification of speed and power dissipation.

W/L_{Load}	W/L_{Driver}	Speed	Power
1:1	4:1	Highest	Maximum
1:2	2:1	High	Moderate
1:4	1:1	Low	Minimum

For this design we will take ratio W/L_{Load} as 1:2 and W/L_{Driver} as 2:1. For stacked transistor this ratio is kept 4:1.

Stick diagram representation of the circuit is shown in Fig. 3.3.

Device count = 7 (including 2 depletion type transistors)

Height and length of the cell can be estimated directly from stick diagram.

Estimated height = 38 λ

Estimated length = 37 λ

Layout is prepared following the process and drain rules as given by Mead and Conway [2]. Layout is shown in Fig. 3.4. We shall now calculate the parasitic capacitance at various nodes and estimate the rise and fall times at these nodes.

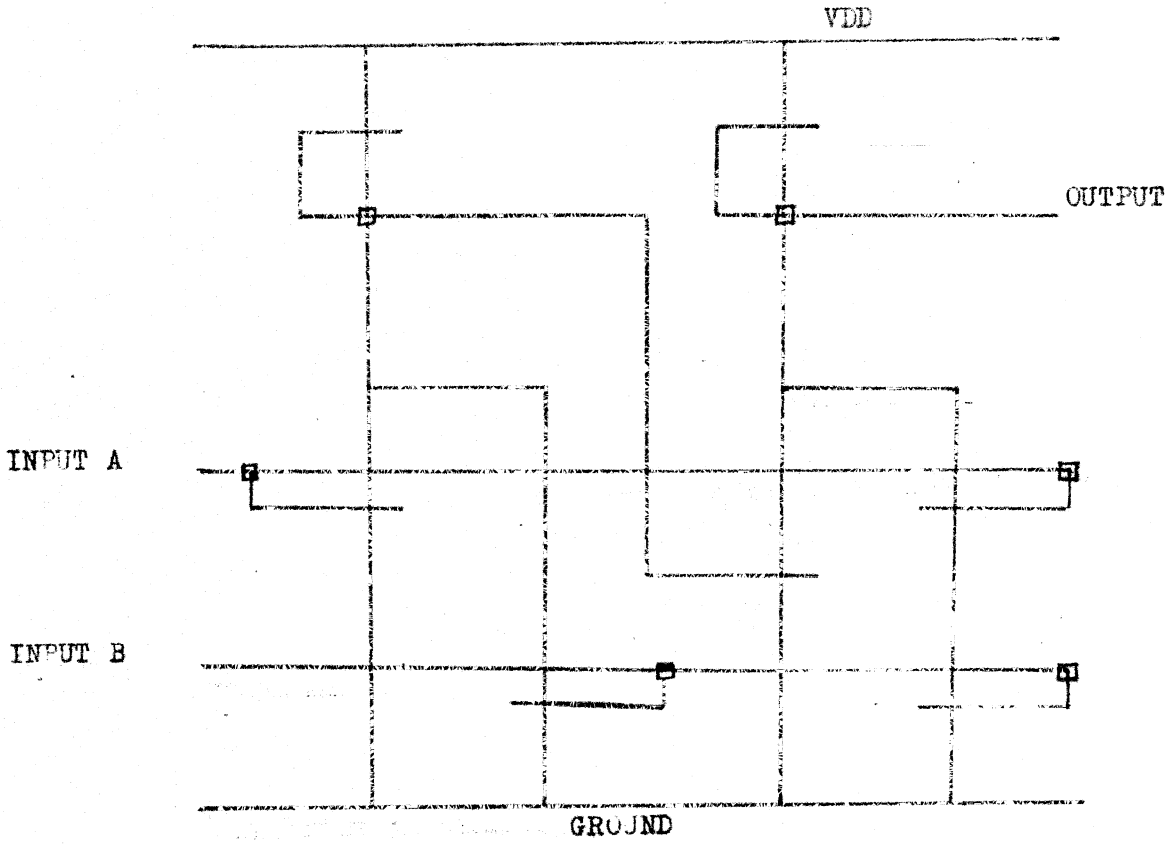


FIG. 3.3. STICK DIAGRAM REPRESENTATION OF THE EXCLUSIVE-OR GATE

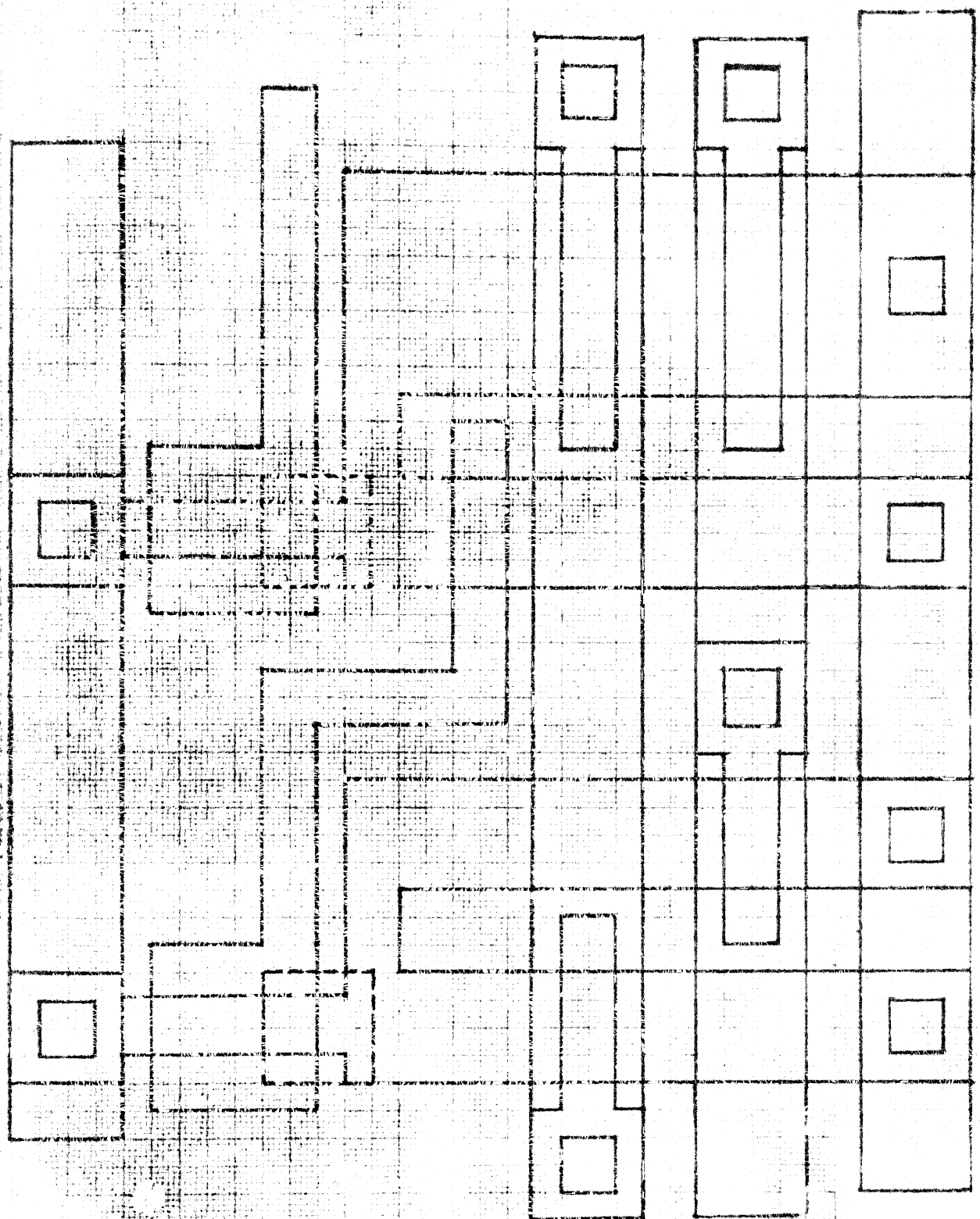


FIG. 3·4 LAYOUT SCHEMATIC OF EXCLUSIVE-OR GATE

Fan-out of the NOR gate is one, i.e. it has to drive the gate of only one transistor and it's interconnection.

Area of polysilicon track $= 18\lambda \times 2\lambda = 36\lambda^2$

Area of the gate $= 8\lambda^{2a}$

Total capacitance $C_A = 36 \times 4 \times 4 \times 10^{-5} + 8 \times 4 \times 4 \times 10^{-4}$

$= 0.01856$ PF

Similarly load at the output node consist of capacitance of polysilicon track.

Area of polysilicon track $= 14\lambda \times 2\lambda = 28\lambda^2$

Total capacitance $C_B = 28 \times 4 \times 4 \times 10^{-5}$

$= 4.48 \times 10^{-3}$ PF

Using the following approximate relationship for rising and falling times

$T_{Rising} = 60 \left(\frac{L}{W}\right)_{Load} \times C_{Node}$

$T_{Falling} = 27 \left(\frac{L}{W}\right)_{Driver} \times C_{Node}$

$T_{A\ Rising} = 2.227$ ns

$T_{A\ Falling} = 0.2505$ ns

$T_{B\ Rising} = 0.5376$ ns

$T_{B\ Falling} = 0.0604$ ns

3.3 STRUCTURED LOGIC (PLA) [2,9,18]

So far we have discussed in detail about the Inverter, NOR and NAND with their different configurations. And also we designed layouts for such premitive cells. Progressing in the same direction we then designed some circuits to perform the logic functions of relatively higher complexity (For example Exclusive-OR) in random logic. While designing the circuits of increasingly higher functional complexity, we experienced it that as the number of output functions increases it becomes more and more difficult to optimize the number of transistors and also the logic design is no longer systematic. During the design, if it is needed to add or modify some output function then, it is almost equivalent to redesigning of the full circuit. Overall design time in random logic to considerably long for larger circuits.

The programmable logic array (PLA), ensures correct design of combinational/sequential circuits and which is highly systematic in nature. Design with this logic can enormously cut-down the design time from months to days or hours. PLA can be considered as a special case of ROMs. Since it does not contain entries for all possible minterm, it is usually for more compact than ROM implementation of the same function. For this reason we will restrict our discussion to PLA only.

Any specific PLA structure contains a row of selectively placed transistors (whose gates are controlled by inputs) only for each of those product terms that are actually required to implement a given logic function. The array which contains these row to produce product terms is termed as AND plane. PLA structure also contains a column of selectively placed transistors (whose gates are controlled by 'product lines') only for each of the output function. The array which contains these columns to produce sum of product form of output function is termed as OR plane.

In general number of vertical lines in the PLA

= Number of inputs x 2 + Number of output functions

Number of Horizontal lines

= Total number of product terms required to synthesis the output functions.

The input register bit is formed by a pair of inverting/non-inverting super buffers. Input/output buffers are required to drive long (capacitive)lines. Though each plane basically performs a NOR operation but functionally we observe that AND plane produces the product terms and OR plane OR's them together to form the output function.

The overall shape and size of a PLA is a function of the following parameters.

(a) Number of inputs

(b) Number of product terms

(c) Number of output functions

(d) The process dependent factor .

If number of inputs/outputs can be reduced then some saving in length of PLA can be achieved. However, generally it is not possible to reduce the number of inputs/outputs. Minimization of number of (product) terms in a function is not as important as minimization of the total number of different multi-output prime implecants. The cost of minimizing the function should be evaluated and justified against the gain in performance and saving in silicon area.

Sequential circuits can also be implemented on PLA by providing an appropriate feedback from the output to the input through some suitable delay unit. Direct feedback may lead to race-around condition.

3.3.1 Full Adder

To illustrate the concepts of structured logic design, a full adder cell has been designed using PLA. Logical functional specification of a full adder circuit is given below.

Inputs			Outputs	
Carry in C_{i-1}	Addend A_i	Augend B_i	Sum S_i	Carry out C_i
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Expression for sum and carry can be derived as

$$SUM = \overline{C}\ \overline{A}\ B + \overline{C}\ A\ \overline{B} + C\ A\ B + C\ \overline{A}\ \overline{B}$$

$$CARRY = \overline{C}\ A\ B + C\ \overline{A}\ B + C\ A\ \overline{B} + C\ A\ B$$

after simplification using Karnaugh map yields

$$SUM = AC + BC + AB + ABC$$

$$CARRY = AB + BC + CA$$

where A and B are bits to be added and C is the carry from previous stage. 'SUM' and 'CARRY' are sum and carry output respectively.

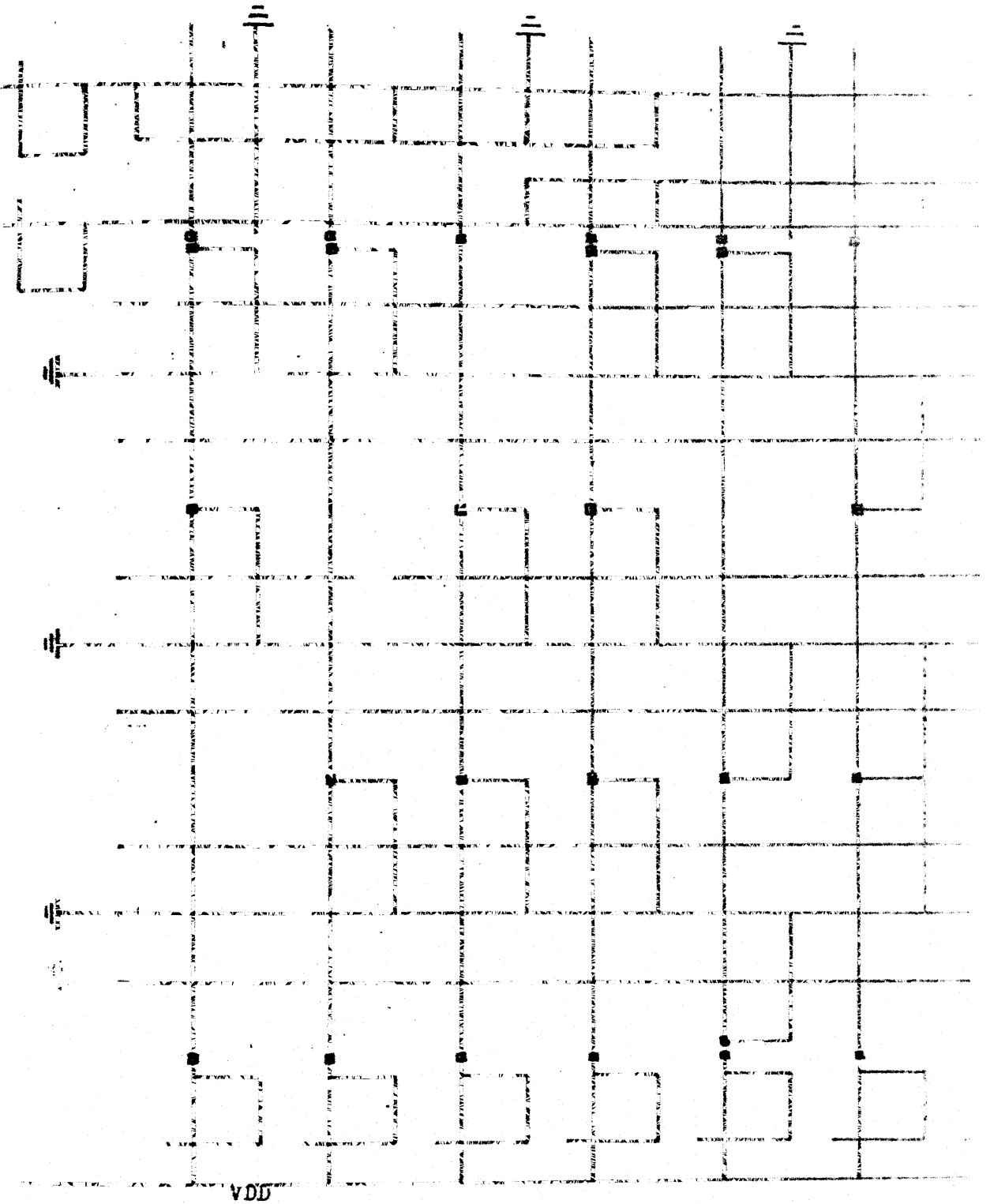


FIG. 3.5 STICK DIAGRAM REPRESENTATION OF FULL ADDER IMPLEMENTED USING PLA

IMPLEMENTED ON PLA * (ONE BIT ONLY)

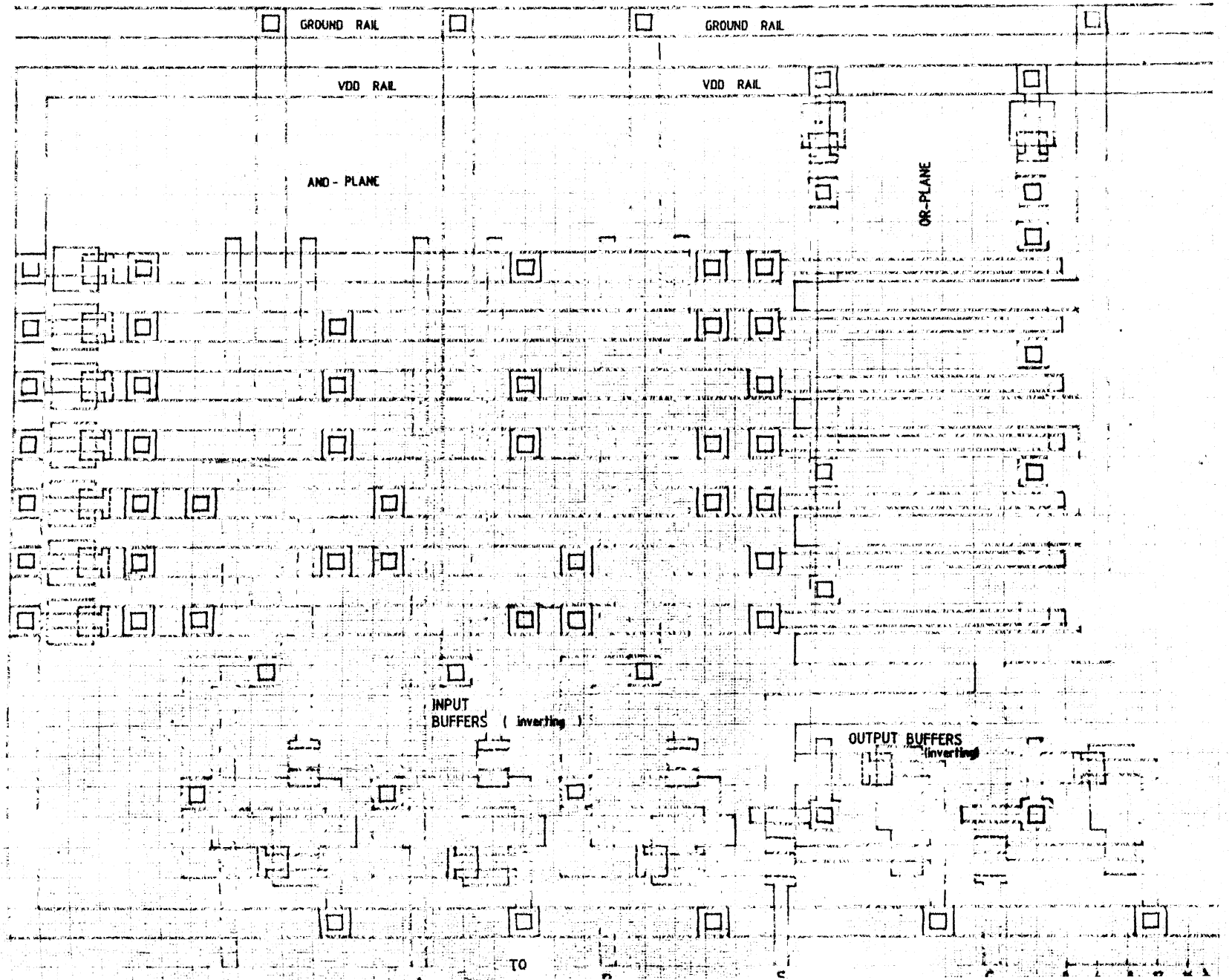


Fig. 3.6

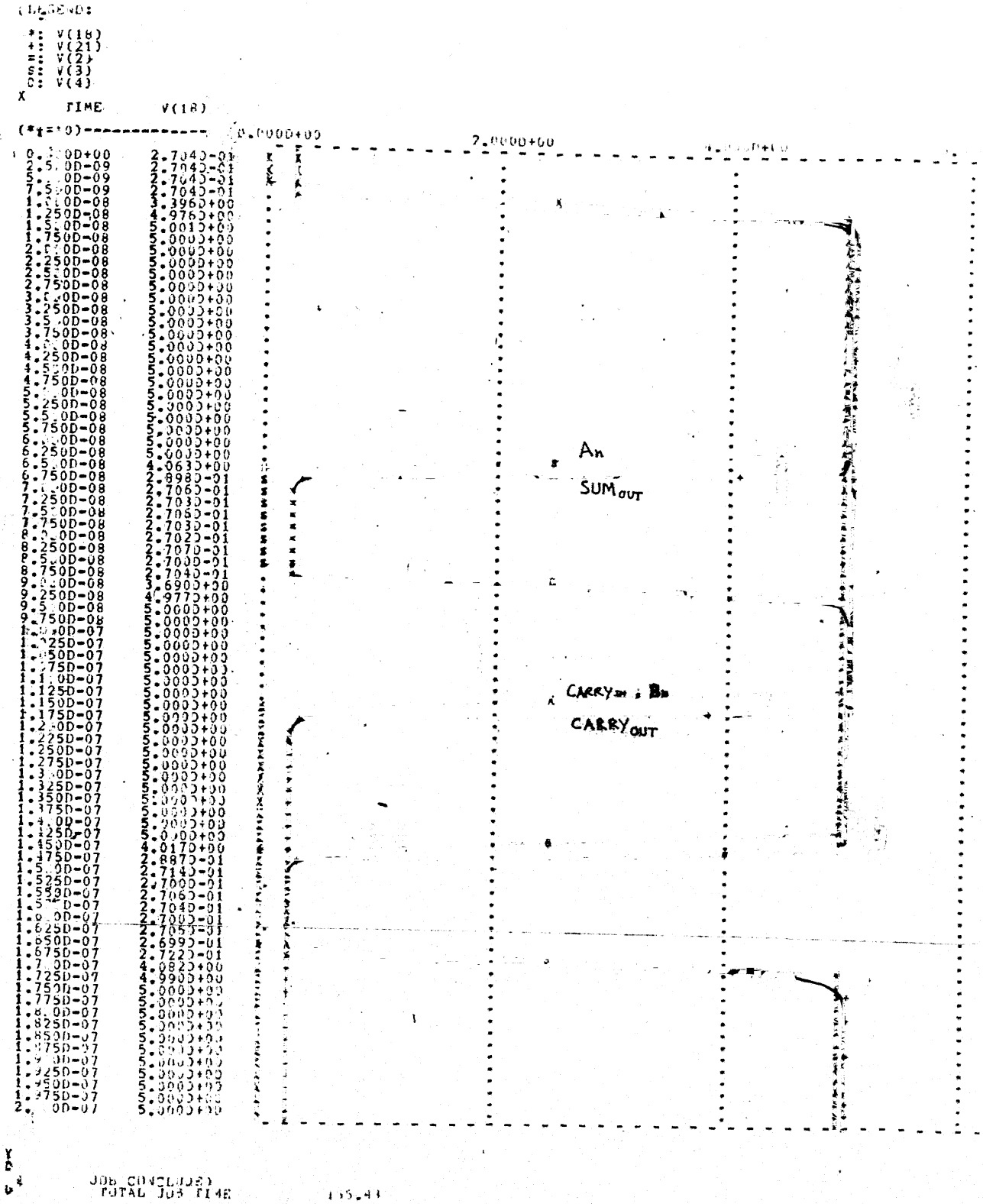

LEGEND:
*: V(18)
+: V(21)
=: V(2)
S: V(3)
D: V(4)
TIME
V(18)
An
SUM OUT
CARRY IN ; Bn
CARRY OUT

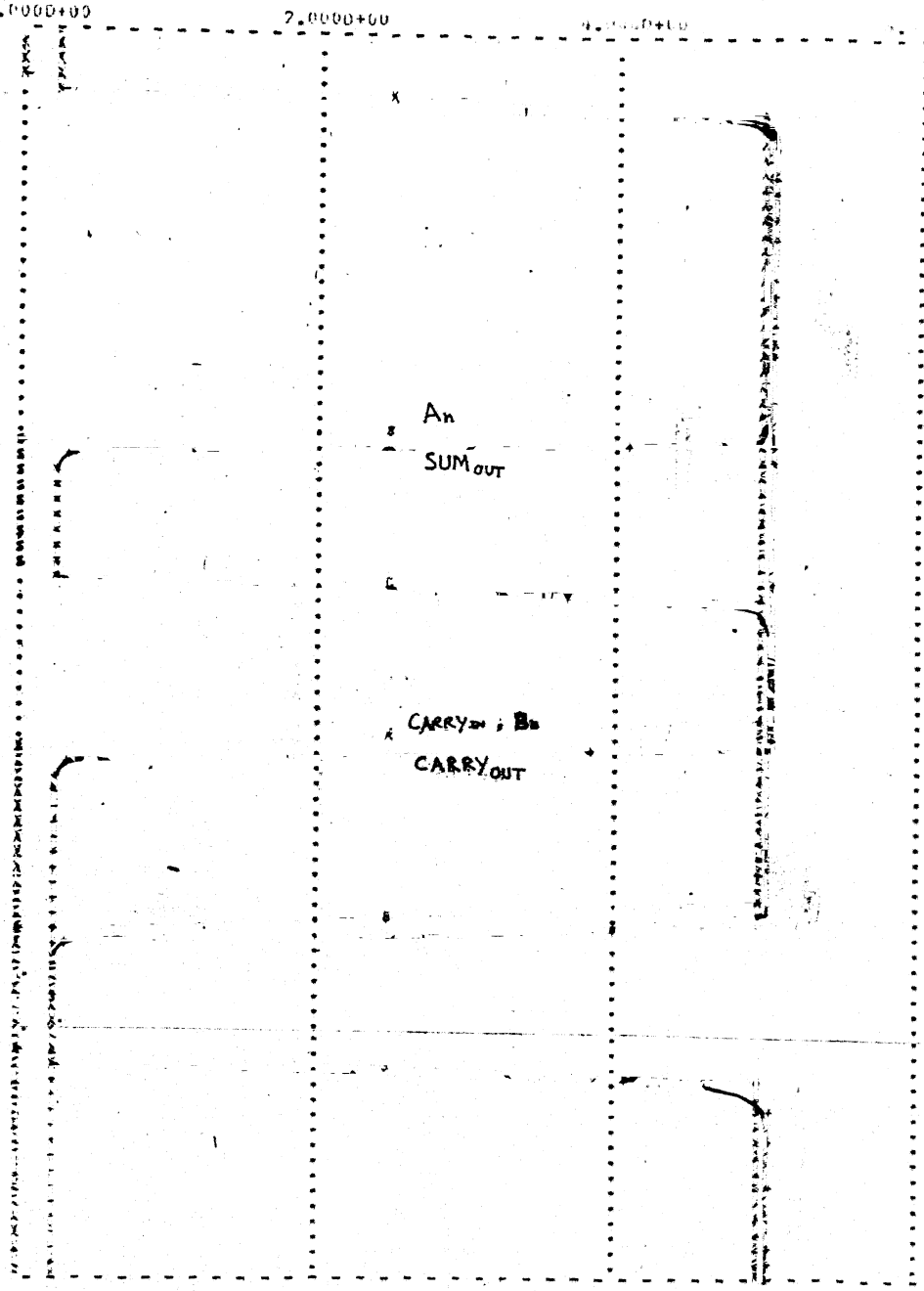
FIG. 3.7

LEGEND:

*: V(18)
+: V(21)
=: V(2)
s: V(3)
0: V(4)

X

TIME	V(18)
0.2[illegible]0D+00	2.7040-01
2.5[illegible]0D-09	2.7040-01
5.[illegible]0D-09	2.7040-01
7.5[illegible]0D-09	2.7040-01
1.0[illegible]0D-08	3.3960+00
1.250D-08	4.9760+00
1.5[illegible]0D-08	5.0010+00
1.750D-08	5.0000+00
2.0[illegible]0D-08	5.0000+00
2.250D-08	5.0000+00
2.5[illegible]0D-08	5.0000+00
2.750D-08	5.0000+00
3.0[illegible]0D-08	5.0000+00
3.250D-08	5.0000+00
3.5[illegible]0D-08	5.0000+00
3.750D-08	5.0000+00
4.0[illegible]0D-08	5.0000+00
4.250D-08	5.0000+00
4.5[illegible]0D-08	5.0000+00
4.750D-08	5.0000+00
5.0[illegible]0D-08	5.0000+00
5.250D-08	5.0000+00
5.5[illegible]0D-08	5.0000+00
5.750D-08	5.0000+00
6.0[illegible]0D-08	5.0000+00
6.250D-08	5.0000+00
6.5[illegible]0D-08	4.0633+00
6.750D-08	2.8980-01
7.0[illegible]0D-08	2.7060-01
7.250D-08	2.7030-01
7.5[illegible]0D-08	2.7060-01
7.750D-08	2.7030-01
8.0[illegible]0D-08	2.7020-01
8.250D-08	2.7070-01
8.5[illegible]0D-08	2.7000-01
8.750D-08	2.7040-01
9.0[illegible]0D-08	3.6900+00
9.250D-08	4.9770+00
9.5[illegible]0D-08	5.0000+00
9.750D-08	5.0000+00
1.0[illegible]0D-07	5.0000+00
1.025D-07	5.0000+00
1.050D-07	5.0000+00
1.075D-07	5.0000+00
1.1[illegible]0D-07	5.0000+00
1.125D-07	5.0000+00
1.150D-07	5.0000+00
1.175D-07	5.0000+00
1.2[illegible]0D-07	5.0000+00
1.225D-07	5.0000+00
1.250D-07	5.0000+00
1.275D-07	5.0000+00
1.3[illegible]0D-07	5.0000+00
1.325D-07	5.0000+00
1.350D-07	5.0000+00
1.375D-07	5.0000+00
1.4[illegible]0D-07	5.0000+00
1.425D-07	5.0000+00
1.450D-07	4.0170+00
1.475D-07	2.8870-01
1.5[illegible]0D-07	2.7140-01
1.525D-07	2.7000-01
1.550D-07	2.7060-01
1.5[illegible]0D-07	2.7040-01
1.6[illegible]0D-07	2.7000-01
1.625D-07	2.7050-01
1.650D-07	2.6990-01
1.675D-07	2.7220-01
1.7[illegible]0D-07	4.0820+00
1.725D-07	4.9900+00
1.750D-07	5.0000+00
1.775D-07	5.0000+00
1.8[illegible]0D-07	5.0000+00
1.825D-07	5.0000+00
1.850D-07	5.0000+00
1.875D-07	5.0000+00
1.9[illegible]0D-07	5.0000+00
1.925D-07	5.0000+00
1.950D-07	5.0000+00
1.975D-07	5.0000+00
2.[illegible]0D-07	5.0000+00



Y

JOB CONCLUDED
TOTAL JOB TIME 135.48

FIG. 3.7

A stick diagram representation of the circuit is given in Fig. 3.5. Pull up transistors (i.e., load transistors) in both AND and OR plane are depletion mode transistors. There are seven horizontal metal lines in the AND plane, each corresponding to one product term. Transistors in AND plane or OR plane have same W/L ratio as that of driver transistor in standard inverter. Ouput/input buffers are inverting super buffers. To avoid the complexity only inverting buffer has been considered but in actual practice there will be a pair of inverting and noninverting buffers. Actual layout is shown in Fig. 3.6. For this implementation, logic minimizatic is not considered. Layout rules are followed as described by Mead and Conway. Parameters are extracted from the actual top logy and used in SPICE simulation of full adder cell. The simulated behaviour of the circuit has been found to be excellent, simulated output is shown in Fig. 3.7.

3.4 DYNAMIC LOGIC [10,19]

The representative example of this class is dynamic register. Operation of dynamic circuit depends upon charge storage at the nodes for data retention. If the clock run, too slow or steps then stored data will be lost. Despite this, it offers economy in space & power dissipation. Also dynamic logics are fast. There are a large variety of, ratioless/ ratioed circuit in dynamic logic using 1 clock, 2 clocks 4 clocks etc. (multiphase clocks).

Selection of clock phasing and circuit type depends on many factors for specific system application. As the number of clocks increases, complexity of the circuitry also increases.

3.4.1 Two Phase Ratioless Dynamic Shift Register

To illustrate the concepts of dynamic logic design, complete design of two phase ratioless dynamic shift register cell has been presented. Fig. 3.8 shows the circuit diagram.

Operation : [I] ϕ_1 is high : The input signal state will be sampled through T_{P1} and it is stored in the input node capacitance of T_2 i.e. C_1. T_1 is connected for saturated mode of operation (i.e., gate tied with drain) and therefore maximum voltage at the output node, i.e. source of T_1 will rise upto $(V_{\phi_1}-V_{TH_1})$ and this will be stored in C_2.

[II] ϕ_1 is low : Depending upon the logic stored at the input gate of T_2 (i.e., in capacitance C_1), C_2 will be discharged conditionally. During this period T_1 and T_{P1} will also remain off.

[III] ϕ_2 is high : This will start conducting and charge-sharing will take place between C_2 and C_3 and effectively the same state is transferred to the C_3 from C_2. Otuput voltage across C_4 will also go high upto $(V_{\phi_2}-V_{TH3})$.

(IV) ϕ_2 is Low : Depending upon the state stored at the input node of T_4, C_4 will be conditionally discharged.

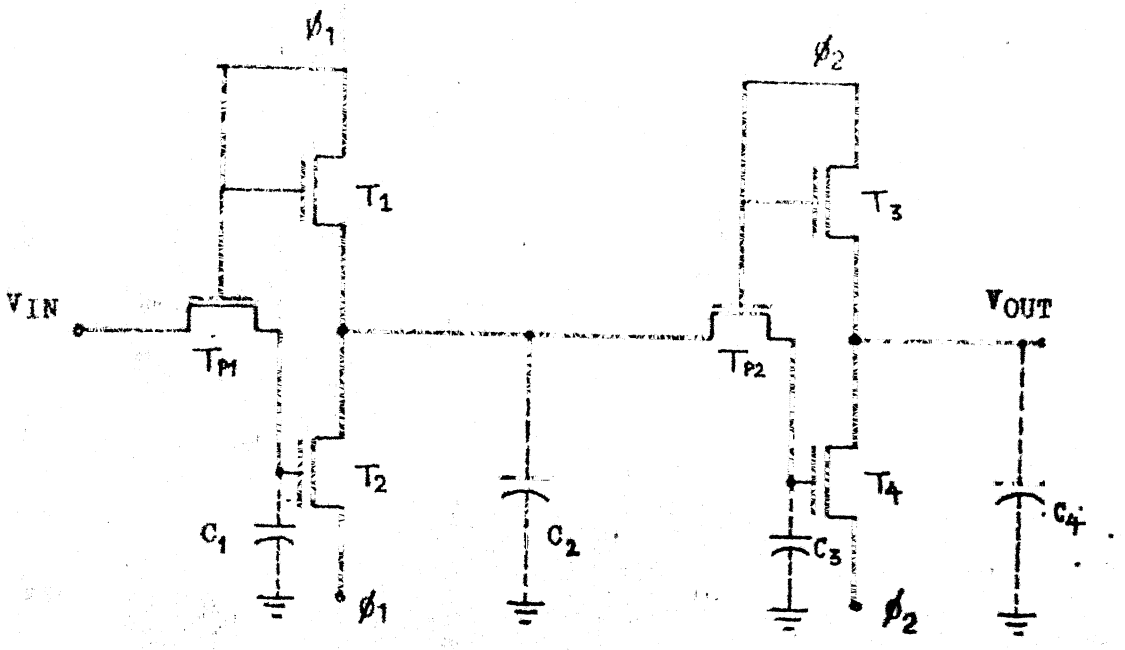


FIG. 3.8.a TWO PHASE RATIOLESS DYNAMIC SHIFT REGISTER CELL

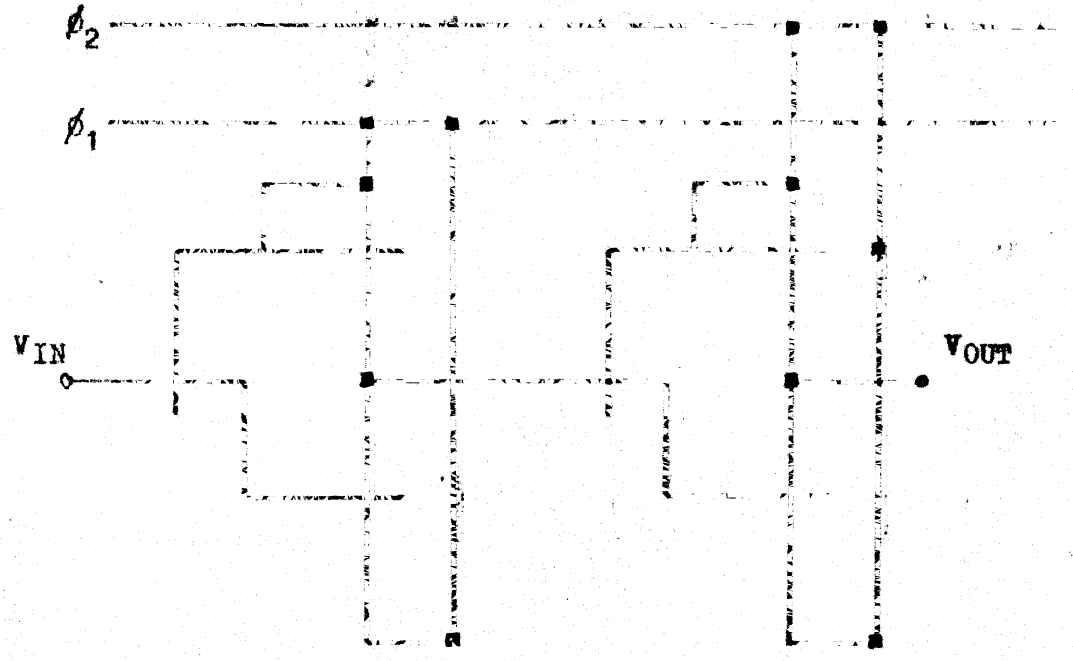


FIG. 3.8.b STICK DIAGRAM OF THE SHIFT REGISTER CELL

Power consumption is $= CV^2f$

where C is clock loading

V is clock voltage

f is clock frequency

Complete layout is shown in Fig. 3.9. This is a modular or regular cell approach. We have designed one bit of the shift register which can be repeated in both the direction, i.e. along and acorss the flow of signal. Clock lines will be across the direction of flow of signal and their number depends upon the number of bit delay in the shift register. One pair of clock lines per bit is needed. Only two clock (metal) rails will be running along the direction of flow of signal. T_1 uses burried contact to connect its gate with drain.

Design of pass transistor is critical, requirements are (1) It should not load clock lines heavily, (2) on resistances should be low. Since pass transistor has to conditionally charge/discharge the input gate node as quickly as possible. To meet this requirement we would like to increase the W/L ratio of the pass transistor. But, then, large geometry transistor will load the clock. During charge sharing, the logic state should not be destroyed. For proper charge-sharing to take place, ratio of capacitance C_2 to C_3 should be around 8-10.

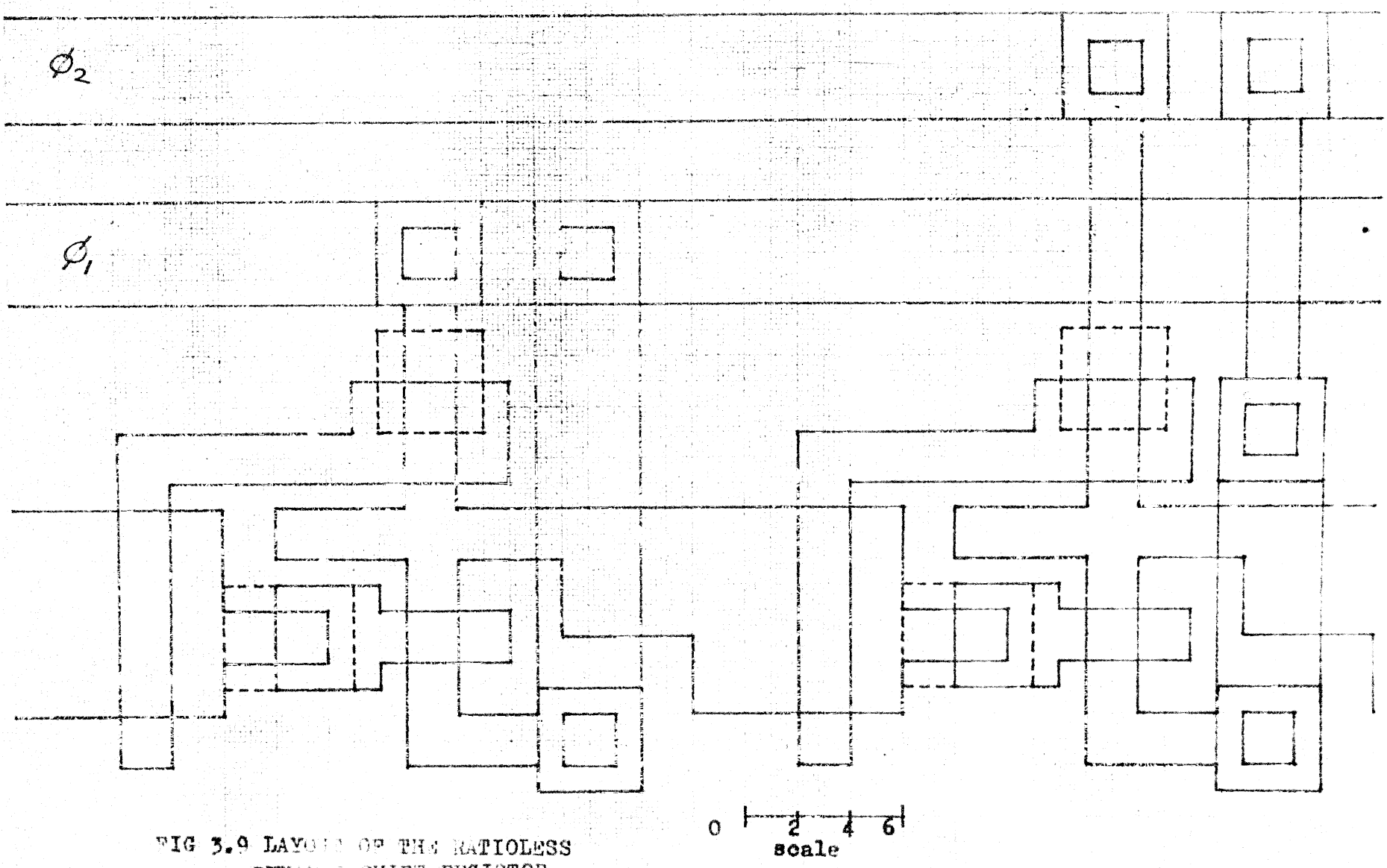


FIG 3.9 LAYOUT OF THE RATIOLESS DYNAMIC SHIFT-REGISTOR

FIG. 3·10

Maximum clock frequency is generally limited by the charging time of the drain of T_2. Minimum clock frequency is limited by the junction leakage current. Excessive leakage current will deteriorate the stored logic levels therefore frequency is to be raised to ensure satisfactory operation. Simulated behaviour of shift register cell is shown in Fig. 3.10.

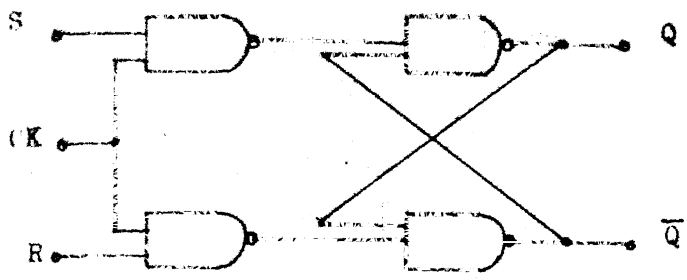
3.5 SEQUENTIAL LOGIC

All the circuits discussed in the preceding sections of this chapter are based upon combinational logic; the outputs at a given instant of time depend only upon the values of the inputs at the same moment. Such a circuit is said to have no memory. Many digital systems require a clock, where each clock pulse advances the digital processing by one step. Output states are obtained in synchronism with the clock.

The output states are not only function of present inputs but also depends upon the previous history. Such a logic is called sequential logic which has a memory to remember its previous history.

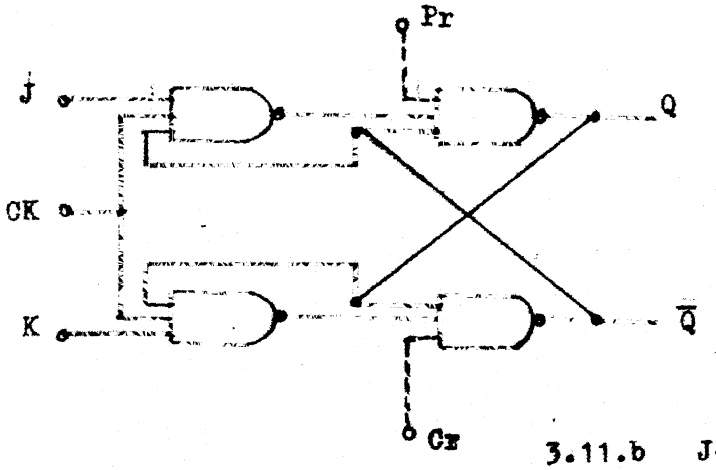
3.5.1 FLIP-FLOPS

In MOS logic, basic memory element can be obtained by cross-coupled inverters. Logic diagram of an S-R clocked flip-flop is shown in Fig. 3.11,a. An S-R flip-flop has one input combination for which output states are undefined. This



Sn	Rn	Qn+1
0	0	Qn
1	o	1
0	1	0
1	1	?

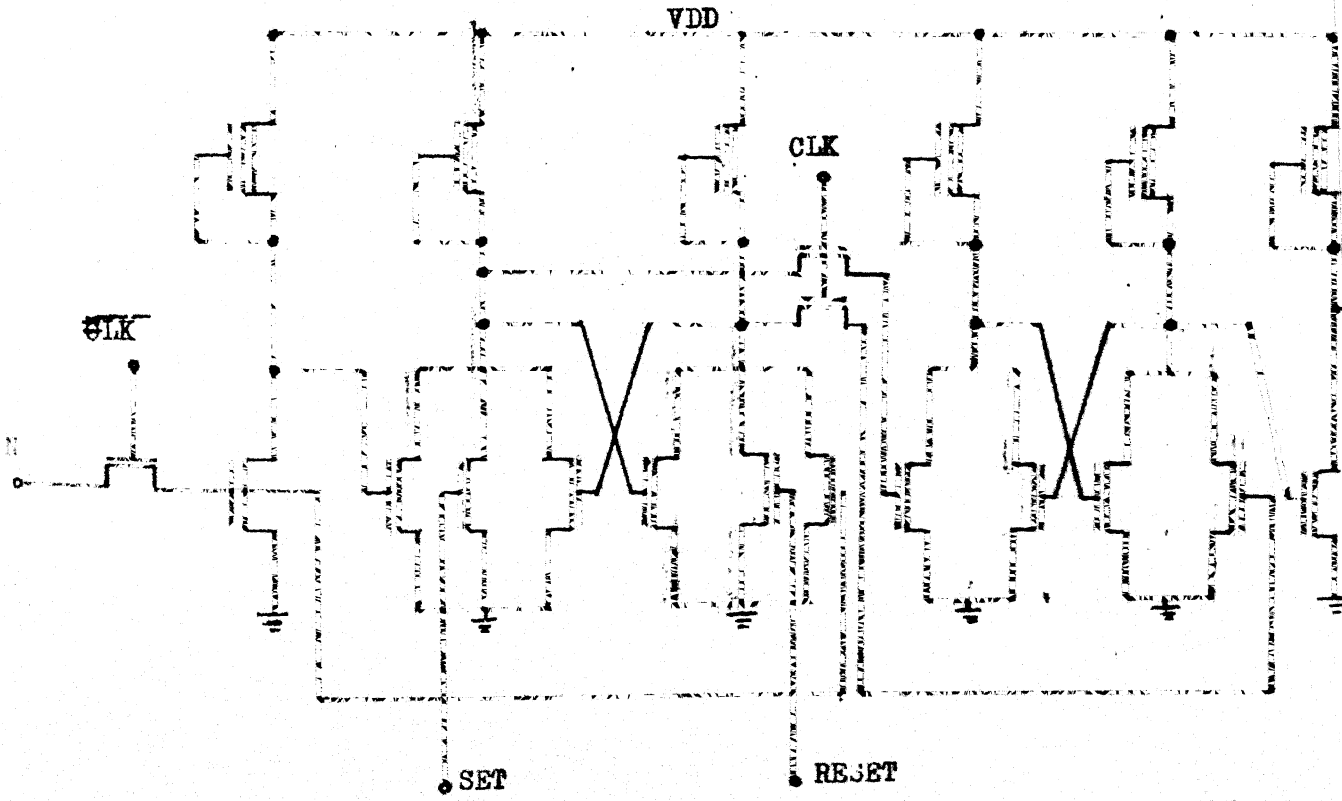
3.11.a CLOCKED R-S FLIP-FLOP



	CK	CR	PR	Q
Enable	1	1	1	*
Clear	0	0	1	0
Preset	0	1	0	1

3.11.b J-K FLIP-FLOP

FIG. 3.11 FLIP-FLOPS



3.11.c CIRCUIT SCHEMATIC OF D-TYPE FLIP-FLOP

ambiguity has been removed in J-K flip-flop shown in Fig. 3.11,b. A master slave J-K flip-flop can be used to avoid race around condition. In T-type flip-flop, output state toggle with each clock pulse. A J-K flip-flop can be converted into a T-type flip-flop if J = K = 1. In a D-type flip-flop, input states will appear at the output only after a delay, determined by clock period. If a J-K flip-flop is modified such that $K = \bar{J}$ then it becomes a D-type flip-flop. We have used D-type flip-flops to provide feedback in a PLA based counter design, described in the next section. For a D-type flip-flop used in the feedback loop in the counter, essential requirements are as follows : When a flip-flop responds to the triggering transition of the clocking waveforms the flip-flop must then find itself in a situation in which it can no longer respond to a further change in input data. It is hence the case that the data present at the input during clock = 0 will be transferred to the output during high going clock edge, at the same time disable the input latch and keep it disabled during the period clock is high. During this period any change in input will not affect output. When clock returns to low ('0') input will be enabled, at the same time output states will be preserved in an isolated output latch.

Keeping these requirement in mind we have designed a D-type flip-flop cell by random approach. Circuit schematic is shown in Fig. 3.11,c. We have used pass transistor switches to

enable/disable the input/output latches. Total number of MOSFETs in the D-flip-flop cell is 21, including six depletion type loads and three pass transistors. Minimum pulsewidth is determined by the time required to transfer the states from input latch to output latch. Output of the flip-flop cannot be taken directly from output latch therefore an inverter is provided to drive the output.

3.5.2 Counter Design Using PLA

The counting function implemented using PLA can be obtained for a variety of fixed or variable modules by using the PLA structure to implement the coincidence detector for states of feedback FF. The PLA counter uses AND plane to sense the present state and to generate the product terms of next state function, OR plane is used to generate next state function for input to feedback flip-flops. Input to AND plane of PLA, may include external control inputs in addition to those outputs provided by the flip-flops. With proper coding of the PLA, counter does the counting (UP/DOWN sequence depends upon the coding of the PLA) in normal binary sequence. The counter may now be interrupted at particular state by coincidence detector. In the next state counter can be forced to any desired count state.

Control functions necessary for sequencing the counter are:

(1) the normal binary incrementing function, f

(2) the external control-data input function, F which forces the flip-flop, to the desired state immediately following the final state.

The required input function to each flip-flop is,

$$I = TF + \bar{T}f$$

where T = minterm of the final state contained within the transition diagram.

The transition sequence diagram for a variable modulo counter in which count advances between the control-data input and 1111 is shown in Fig. 3.12,a.

From the transition diagram and knowledge of the logic function of the D-type (delay) flip-flop, the Karnugh map can be specified for each separate bit as shown in Fig. 3.12.b. Specifically, one Karnaugh map is used for each flip-flop in the feedback array. These 4 bits are specified as WXYZ with Z bit being the least significant bit.

Now, the function f, can be derived for each bit,

$$W^{n+1} = W\bar{X} + W\bar{Y} + W\bar{Z} + \bar{W}XYZ$$

$$X^{n+1} = X\bar{Y} + X\bar{Z} + \bar{X}YZ$$

$$Y^{n+1} = \bar{Y}Z + Y\bar{Z}$$

$$Z^{n+1} = \bar{Z}$$

and minterm of the final state, T, contained within the transition diagram is,

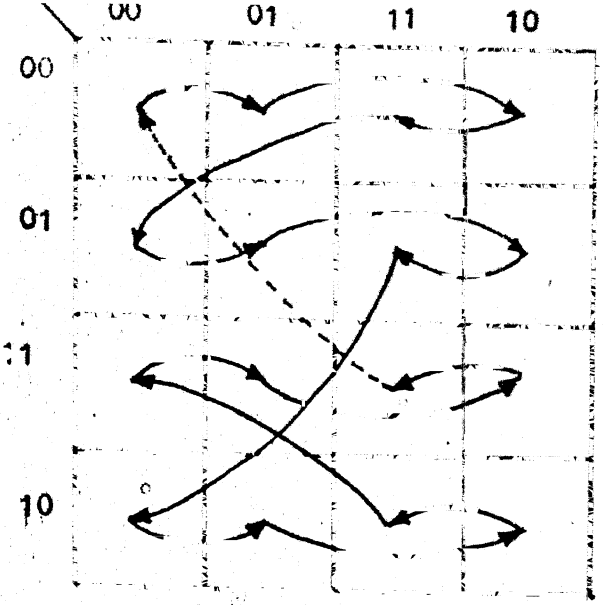


FIG 5.12, a TRANSITION SEQUENCE DIAGRAM

0	0	0	0
0	0	1	0
1	1	0	1
1	1	1	1

W^{n+1}

0	0	1	0
1	1	0	1
1	1	0	1
0	0	1	0

X^{n+1}

0	1	0	1
0	1	0	1
0	1	0	1
0	1	0	1

Y^{n+1}

1	0	0	1
1	0	0	1
1	0	0	1
1	0	0	1

Z^{n+1}

(b) NEXT STATE FUNCTION FOR EACH FLIP-FLOP

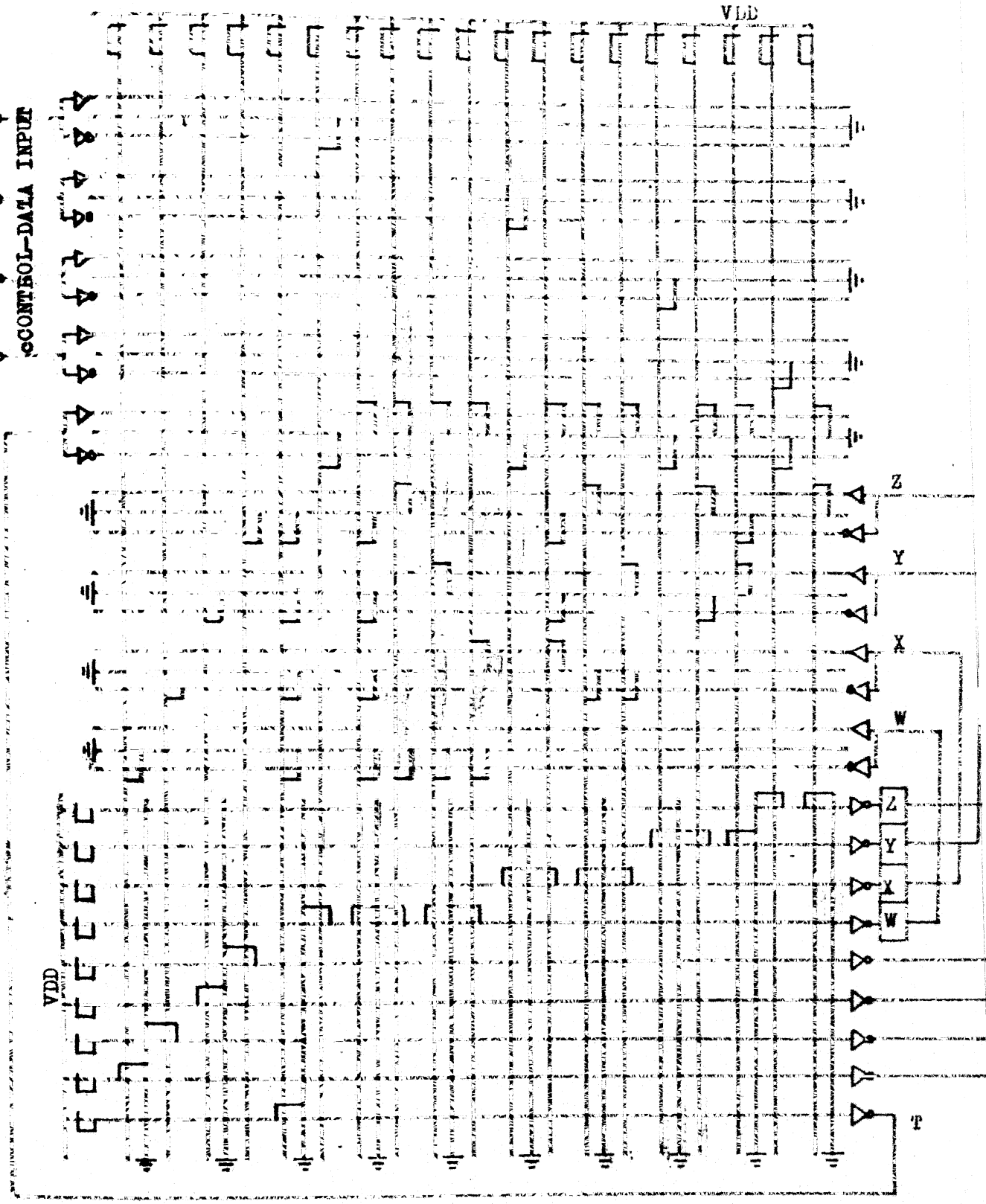


FIG. 3.13 PLA BASED VARIABLE MODULO COUNTER
(RESET TO CONTROL-DATA INPUT)

$$T = WXYZ = 1111$$

We define the external control-data input function F as

$$F = ABCD$$

input to each flip-flop can be expressed as

$$I = TF + \bar{T}f$$

$$W_d^{n+1} = \bar{T}W\bar{X} + \bar{T}W\bar{Y} + \bar{T}W\bar{Z} + \bar{T}WXYZ + TA$$

$$X_d^{n+1} = \bar{T}X\bar{Y} + \bar{T}X\bar{Z} + \bar{T}\bar{X}YZ + TB$$

$$Y_d^{n+1} = \bar{T}\bar{Y}Z + \bar{T}Y\bar{Z} + TC$$

$$Z_d^{n+1} = \bar{T}\bar{Z} + TD$$

The expressions above represent next-state functions and will be used for coding the PLA. For instance, the input to the W flip-flop consists of five separate sum terms, specifically, $\bar{T}W\bar{X} + \bar{T}W\bar{Y} + \bar{T}W\bar{Z} + \bar{T}WXYZ + TA$. Coading of PLA is done in the usual manner. Initial states of the flip-flop, after bringing the power on, is determined by control-data input. Stick diagram schematic of the counter based on PLA is shown in Fig.3.13. D type flip-flops are of master-slave type as discussed in Section 3.5.1. Count-out, T, is directly feedback to AND-plane as it can't cause race-around. If ABCD input is 0111 (^{7}10), counter is modulo ^{9}10 counter and count advances between 0111 and 1111.

3.6 CIRCUIT DESIGN WITH MOS [9]

We have already discussed the design of MOS logic circuits. In this section we will study the general form of MOS circuits to realize complex functions. Examples of such form of MOS circuit are adders, counters and memory structure, etc.

3.6.1 Adder

An adder is a logic circuit which performs binary addition of two binary numbers. If the maximum number of bits in the input number is N then the adder is said to be N-bit adder. A half adder only performs half of the addition process, that is, it generates the sum and carry (to be used by next cell) but does not accept any carry. A full-adder, however accepts carry also. Obviously a half adder can be used for LSB addition only while full-adder is necessary for higher significant bits.

There are two methods of arranging full-adders for addition of multibit numbers.

(a) Serial Mode : In this method only one bit full adder is used repeatedly with different pairs of corresponding bits in two numbers to be added. The carry so generated in the process of addition will be stored in the latch and then fedback to full adder for subsequent addition (with pair of bits of next position). Sum is stored in a register. Block diagram of full adder arranged in serial mode operation is shown

in Fig. 3.14. For N-bit adder the length of input/output register will be N+1. CARRY LATCH can also be a D-flip-flop which introduces one bit delay. Output can be obtained serially from the output register. After addition input numbers will be lost, and only sum will be available. To avoid this, Input register can be made recirculating. However, then, some control circuitary is needed to indicate the moment when valid output is available and to enable output register to be read for further operations. Advantage of serial mode of addition is that a considerable saving in area as only one bit full adder is needed. But addition process is slow.

(b) Parallel Mode : In this method, there are N full adders placed in parallel with carry input connected to carry output of the previous bit full adder cell. It also called ripple-carry adder. Sum can be obtained in parallel/serial fashion from the output register. Block diagram is shown in Fig.3.15.

Maximum delay in the parallel adder can be equal to N times the delay of one full adder cell plus delay of last MSB adder. It is necessary to allow some time for addition greater than this maximum delay. Thus it requires fixed time for addition regardless of actual carry propagation characteristic. Other method for fast addition process are carry-look ahead. In this, there is an additional circuitary to examine the data simultaneously and generates carry (if any) for the different position bit adders. This circuit is faster than ripple-carry adder

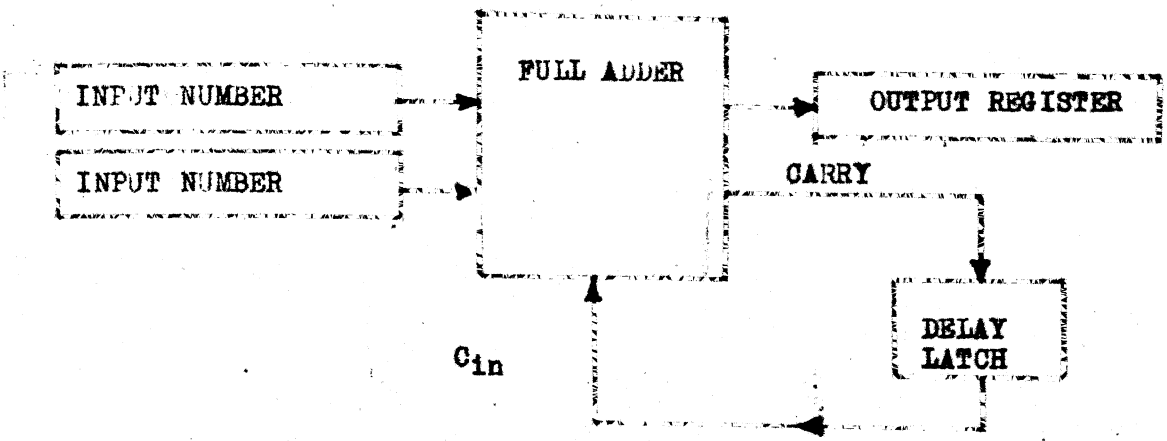


FIG. 3.14 SERIAL ADDER

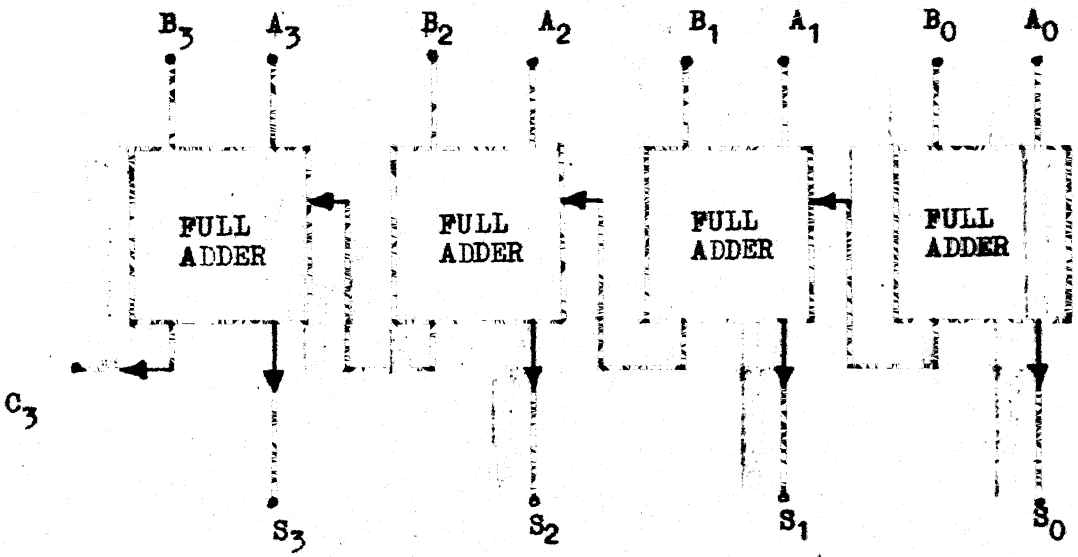


FIG. 3.15 RIPPLE CARRY ADDER

since the whole addition process takes place in two cycles only. In the first cycle carry generator generates the proper carry for the adders, and in next cycle all the adders adds the two bits of corresponding position in the input and process the carry input also. Output is stored in the output register. Again, this is also a fixed time addition process regardless of numbers to be added. One serious drawback of this arrangement is that as the number of bits in the adder increases complexity of additional circuitary increases rapidly and it consumes a considerable area of the chip.

Binary subtraction can also be done using an adder. Normally subtraction is done by adding the 2's complement of the subtrahend, to the number (from which it is to be subtracted).

3.6.2 Counters

In the category of asynchronous counters one arrangement is shown in Fig. 3.16. This counter uses T-flip-flop as basic functional block. Since toggle input to each flip flop is 1, output state toggles on each rising edge of clock input. Toggle output becomes clock input to the next flip-flop.

But this form of counter (realized by T flip-flop) have a long cascade delay. Also during the ripple of output of one stage which also the input to the next stage, false states could be introduced. And it need some decader at output to

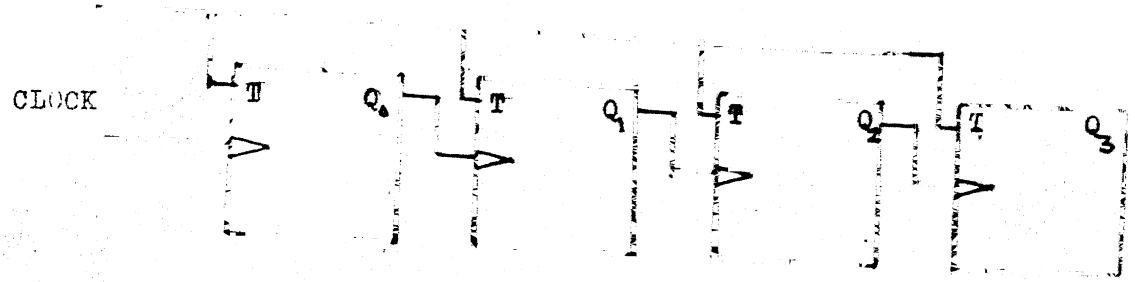


FIG. 3.16 COUNTER BASED ON TOGGLE FLIP-FLOP

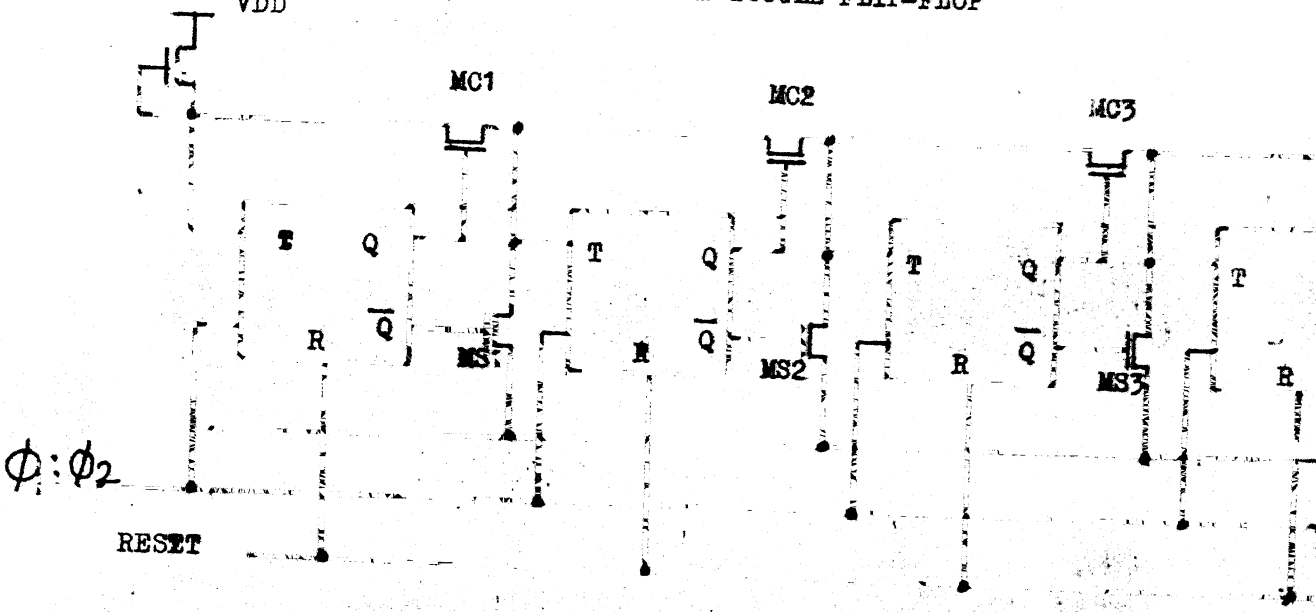


FIG. 3.17 SYNCHRONOUS COUNTER BASED ON TOGGLE FLIP-FLOP (USING PRECHARGE)

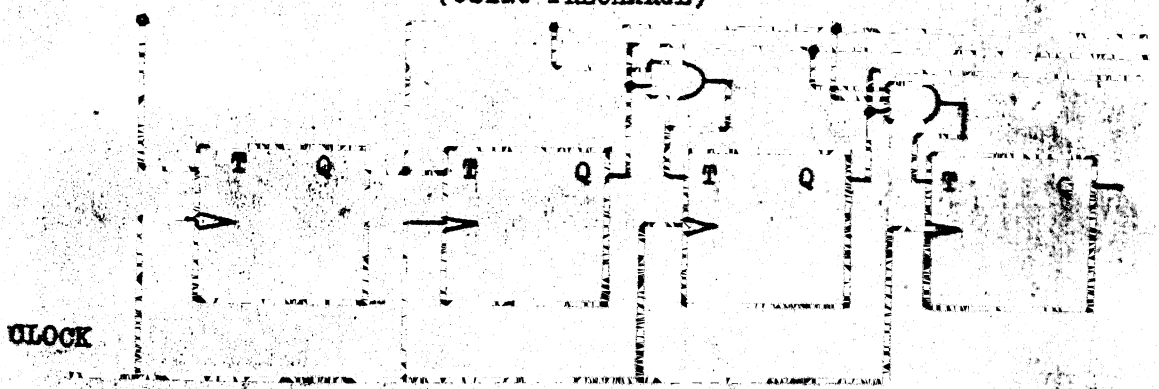


FIG. 3.18 PARALLEL CARRY SYNCHRONOUS COUNTER USING TOGGLE FLIP-FLOP

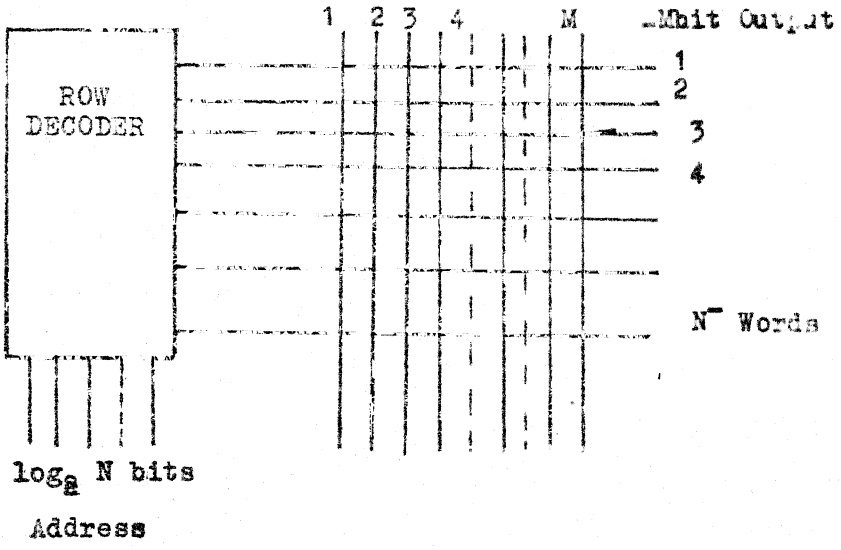


FIG. 3. 9 ROM STRUCTURE

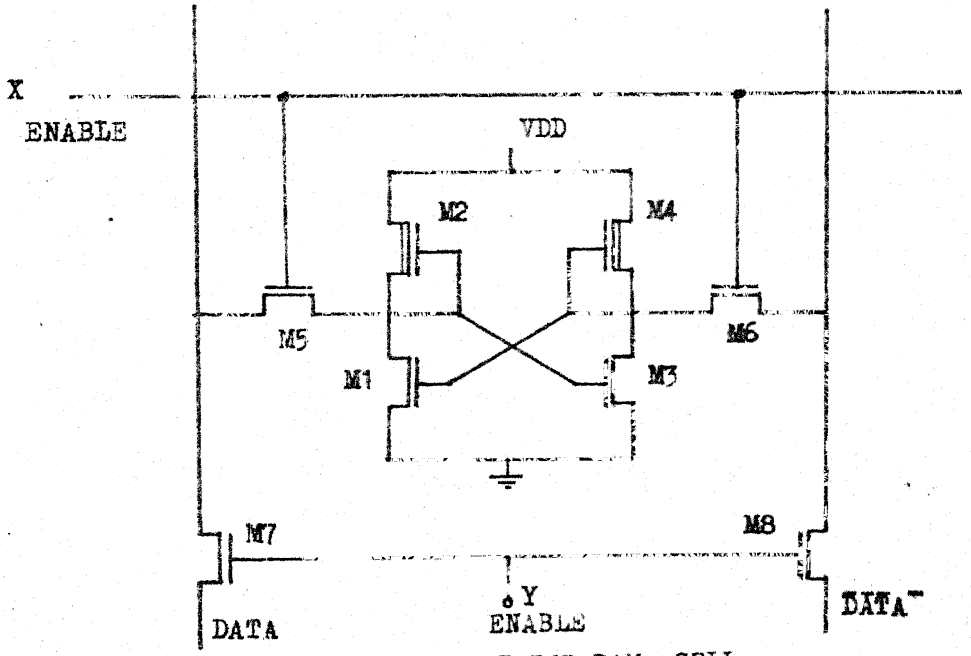


FIG . 3.20 A SIX TRANSISTOR RAM CELL

define the valid states. Typical speed of 4 bit binary counter based on this scheme is around 200 ns.

A synchronous counter is shown in Fig. 3.17.

It requires a two phase clock which is common to all toggle cells. Input and output of each is fed to the toggle input of the next toggle cell through a AND gate. AND gate is realized by pass transistors in C_n and precharge arrangement. If at any stage output of a cell becomes zero then input to next cell would float and it can assume any value. Therefore, to avoid this, shunt transistor MS_n are included in circuit.

This counter derives T input serially through AND gates hence its speed is limited mainly due to AND gates. Typically for a 4 bit counter, speed is around 80 ns.

Another form of circuit for counter is shown in Fig. 3.18.

It is called parallel-carry synchronous binary counter. Since carry is generated in parallel it is fast in operation. Typical maximum delay in 4 bit counter is 60 ns. However, it is not suited for larger bit counters because number of input to AND gate increases very rapidly.

3.6.3 MEMORY

Memory is most vital part of any digital computing system. Memories can be broadly classified as Random Access Memory (RAM) and Read Only Memory (ROM). Again both class can be subdivided into static or dynamic memory.

ROM : Basic ROM structure is shown in Fig. 3.19. Address decoder is actually an AND plane, having N output and $\log_2 N$ bit input address. To generate a 0 at the particular bit of output word, a transistor will be placed with it gate controlled by row enable/select line, and drain aconnected to the output column (bit). Similarly to generate a logic 1 in the cell, transistor is omitted. A dynamic ROM employs precharging for enhancement and therefore it is faster than previously described static ROM which uses active ~~of~~ pull up operation instead.

RAM : This is an array of memory cells in which digital word can be stored and read from an address with proper control signals. It is frequently termed as scrach pad when other control peripherals are added. Density of the RAM depends upon the number of transistor used in one cell of RAM. Typically a RAM cell contain six transistors. It is basically a flip-flop circuit whose Q and $\overline{Q}$ prints can be accessed through the two pair of pass transistors which are controlled by the column and row select lines of the cell. Circuit schematic is shown in Fig. 3.20. To reduce the power dissipation in the cell the depletion type load can be replaced by ion-implanted polysilicon resistances of high value.

CHAPTER 4

SIMULATION OF MOS ICs

Circuit simulation is a very important step in design of Integrated systems. By circuit simulation one can predict the performance of the circuit before actual fabrication, it also helps designer to readjust the parameters to meet the specified performance. Degree of accuracy in prediction of performance depends upon the accurate modelling of the device and correct choice of parameters for the simulation. Out of many simulators available we have used SPICE extensively in our work. SPICE is a general-purpose circuit simulation program for d.c., ac and transient analysis. SPICE allows circuits containing resistors, capacitors, inductors, mutual inductors, independent/dependent four types of sources and some commonly used semiconductor devices. Here we will discuss only that part of SPICE which is relevant to MOS ICs.

SPICE uses built-in models for MOSFET and user have to specify only parameters of the model of the device. Some of the MOSFET models used in the SPICE have been discussed to help the user in choosing correct set of parameter and to understand the limitations of SPICE. An interactive computer program has been developed for accurate evaluation of SPICE MOSFET parameters User has only to furnish few information, on the basis of that,

rest of the parameters will be calculated by the program. This improves the accuracy of simulation considerably and gives greater flexibility to the SPICE user.

4.1 CIRCUIT SIMULATION USING SPICE [20]

SPICE offers following types of analysis of the circuits.

D.C. Analysis : The d.c. analysis portion of SPICE determines the d.c. operating point of the circuit with capacitors open inductors shorted. A d.c. analysis is automatically performed prior to a transient analysis to determine the transient initial conditions. It can also be used to generate d.c. transfer curves, in this case, a specified independent voltage or current source is stepped over a user-specified range and the d.c. output variable are stored for each sequential source value. The d.c. analysis options are specified in .DC control statement discussed later.

A.C. Small Signal Analysis : The a.c. small-signal portion of the SPICE computes the a.c. output variable as a function of frequency. The program first computes the d.c. operating point and then determines the linearized model of the nonlinear device in the circuit. The resultant circuit is then analyzed over a specified range of frequencies. The a.c. small-signal analysis options are specified in .AC control statement.

Transient Analysis : The transient analysis portion of SPICE computes the transient output variables as a function of time over a user specified time interval. The initial conditions are automatically determined by a d.c. analysis. The transient analysis time intervals are specified on the .TRAN control statement.

Analysis at Different Temperatures : All input data for SPICE is assumed to have been measured at 27 deg. C (300 deg. K), The simulation also assumes a nominal temperature of 27 deg. C. The circuit can be simulated at other temperatures by using a TEMP control statement. Temperature appears explicitly in the value of junction potential ϕ, and surface mobility μ, for MOSFET model. Threshold voltage and reverse saturation currents of the junction are strong function of temperature. Utilizing this facility of SPICE, one can examine the circuit performance at any temperature. This facility will enable us to determine the circuit reliability at elevated temperature. Temperatures less than -223.0 deg. C are ignored. General form of the Temp control statement is

. TEMP T_1 T_2 T_3 ...

where T_1 ,T_2, ... are the temperatures at which simulation is requested.

4.1.1 Input Description

TITLE, COMMENT and .END statements.

(1) TITLE : This statement is the first line in the data. It is printed as heading for each section of output.

EX :-

ONE BIT FULL ADDER CIRCUITON PLA

<Rest of the Input data>

(ii) COMMENT : This statement can be inserted only where in the input data except between continued lines. Comment line starts with an asterisk '*' in the first column.

* Following four statements are for simulating clocks.

(iii) END : This control statement is always the last statement in the input data. Period is an integral part of .END statement.

CIRCUIT ELEMENT STATEMENTS

Capacitors and Resistors : Capacitors and Resistors in the circuit are described as follows.

	CXXXXXXX	N1	N2	VALUE
	RXXXXXXX	N1	N2	VALUE <Te>
	CLOAD	10	12	10PF optional
Exam	RLOAD	10	12	2K

it states that a resistor (capacitor) named RLOAD (CLOAD) is connected between nodes 10 and 12 and its value is 2K (10PF).

MOSFETS : General form of MOSFET description statement is MXXXXXXX ND NG NS NB MNAME <L=VAL><W=VAL> + <AD=VAL> <AS=VAL><PD=VAL><PS=VAL><NRO=VAL><NR =VAL> ND,NG,NS and NB represents node numbers corresponding to drain, gate, source and substrate. L and W are length and width of the channel respectively. AD,AS are areas of drain and source regions respectively. PD, PS are the periphery of the drain and source diffusion regions. NRD, NRS are number of squares in drain and source regions respectively. A set of model parameters are specified in. MODEL statement, MNAME is the name of that MODEL statement.

. MODEL Statement : The .Model statement specifies a set of model parameters that will be used by one or more devices.

General form is

.MODEL MNAME TYPE (PNAME1 = VAL, PNAME2 = VAL ---) MNAME is the model name and TYPE is one of the two, either NMOS or PMOS. Parameter values are defined by appending the parameter name, followed by an equal sign and the parameter value. Model parameters that are not given a value are assigned the default values given below for each model type.

MOSFET Models : SPICE provides three MOSFET device models which differ in the formulation of the I-V characteristic. The variable LEVEL specifies the model to be used.

LEVEL = 1 Shichman-Hodges (square-law I-V characteristic)

LEVEL = 2 MOS2 (An analytical model)

LEVEL = 3 MOS3 (A semiempirical model)

The D.C. characteristics of the MOSFET are defined by the device parameters VTO, KP, LAMBDA, PHI and GAMMA. These parameters are computed by SPICE if process parameters (NSUB, TOX, NSS, ---) are given. Charge storage is modelled by three constant capacitors, CGSO, CGDO and CGBO which represent overlap capacitances, by the nonlinear thin-oxide capacitance which is distributed among the gate, source, drain and bulk regions, and by the nonlinear depletion-layer capacitances for both substrate junctions divided into bottom and periphery, which vary as the MJ and MJSW power of junction voltage respectively, and are determined by the parameters CBD, CBS, CJ, CJSW, MJ, MJSW and PB. There are two built-in models of the charge storage effects associated with the thin-oxide. The default is the piecewise linear voltage-dependent capacitance model proposed by Meyer as discussed in Section 4.2. The second choice is the charge-controlled capacitance model of Ward and Dutton. The XOC model parameter is used as a flag and a coefficient at the same time. If XOC is larger than 0.5 or not defined then Meyer's model will be used else charge-controlled model will be used. In Shichman-Hodges model these voltage dependent capacitances are included only if TOX is specified and they are represented using

J.E. Meyer's formulation. AD,AS,PD,PS is required to determine capacitances and reverse saturation current. NRD, NRS when multiplied by RSH (sheet resistance) give drain and source resistances, but it can directly be given in the model parameters RD and RS.

	Name	Parameter	Units	Default	Example
1.	LEVEL	Model index	-	1	-
2.	VTO	Zero-bias threshold voltage	V	0.0	1.0(Enh)
3.	KP	Transconductance parameter	A/V^2	2.0E-5	3.1E-5
4.	GAMMA	Bulk threshold parameter	$V^{1/2}$	0.0	0.37
5.	PHI	Surface potential	V	0.6	0.65
6.	LAMBDA	Channel length modulation (for level=1 and level=2 only)	1/V	0.0	0.02
7.	RD	Drain ohmic resistance	Ohm	0.0	1.0
8.	RS	Source ohmic resistance	Ohm	0.0	1.0
9.	CBD	Zero-bias B-D junction capacitance	F	0.0	20 fF
10.	CBS	Zero-bias B-S junction capacitance	F	0.0	20 fF
11.	IS	Bulk-junction saturation current	A	1.0E-14	1.0 E-15
12.	PB	Bulk-junction potential	V	0.8	0.87
13.	CGSO	Gate-source overlap capacitance per meter channel width	F/m	0.0	4E-11
14.	CGDO	Gate-drain overlap capacitance per meter channel width	F/m	0.0	4E-11

15. CGBO	Gate-bulk overlap capacitance per meter channel length	F/m	0.0	2.0E-10
16. RSH	Drain and source diffusion sheet resistance	Ohm/sq.	0.0	10.0
17. CJ	Zero-bias bulk junction bottom capacitance per sq. meter of junction area	F/m^2	0.0	2.0E-4
18. MJ	Bulk junction bottom capacitance per sq.meter of junction area	F/m^2	0.0	2.0E-4
19. CJSW	Zero-bias bulk junction sidewall capacitance per meter of junction perimeter	F/m	0.0	1.0E-9
20. MJSW	Bulk junction sidewall grading coefficient	0.33		
21. JS	Bulk junction saturation current per sq.meter of junction area	A/m^2	-	1.0E-8
22. TOX	Oxide thickness	metre	1E-7	1E-7
23. NSUB	Substrate doping	Cm^{-3}	0.0	4E15
24. NSS	Surface state density	Cm^{-2}	0.0	1E10
25. NES	Fast surface state density	Cm^{-2}	0.0	1E10
26. TPG	Type of gate material:(for polysilicon +1/-1 depending upon its doping type) +1 opposite to substrate -1 same as substrate 0 aluminium gate			
27. XJ	Metallurgical junction depth	metre	0.0	1E-6
28. LD	Lateral diffusion	metre	0.0	0.8E-6
29. UO	Surface mobility	$Cm^2/V\text{-}S$	600	600-900

30. UCRIT	Critical field for mobility degradation (MOS2 only)	V/cm	1E4	1E4
31. UEXP	Critical field exponent in mobility degradation (MOS2 only)		0.0	0.1
32. UTRA	Transverse field coefficient (mobility) (deleted for MOS2)		0.0	0.3
33. VMAX	Maximum drift velocity of carriers	m/s	0.0	5E4
34. NEFF	Total channel charge (fixed and mobile) coefficient (MOS2 only)		1.0	5.0
35. XOC	Thin-oxide capacitance model flag and channel charge share attributed to drain(0-0.5)		1.0	0.4
36. KF	Flicker noise coefficient		0.0	1E-26
37. AF	Flicker noise exponent		1.0	1.2
38. FC	Coefficient for forward-bias depletion capacitance formula		0.5	
39. DELTA	Width effect on threshold voltage (MOS2 and MOS3 only)		0.0	1.0
40. THETA	Mobility modulation (MOS3 only)		0.0	0.1
41. ETA	Static feedback (MOS3 only)		0.0	1.0
42. KAPPA	Saturation field factor (MOS3 only)		0.2	0.5

A brief description of these parameter is given in Section 4.2.

. DC Statement :

General form

. DC SPCNAM VSTART VSTOP VINCR (SRC2 START2 STOP2 INCR2)

Example

. DC VDS 0 10 0.5 VGS 0 :5 1

This statement defines the d.c. transfer curve source and sweep limits. SPCNAM is the name of independent voltage source, VSTART, VSTOP, VINCR are start stop and incrementing value of that source respectively. For each value of optinally defined second source, the first source will be swept over its range.

Output Statements :

Results of simulation can be plotted or printed in tabular form. General form of these statement is given below.

. PLOT PLTYPE V(N1) V(N2, N3) ...

where PLTYPE is type of analysis.

DC, TRAN, AC, DISTO etc.

V(N2, N3) is the voltage between node N2 and N3.

All output variables indicated in one PLOT statement will be plotted on the same graph. There is no restriction on number of PLOT statements. For printing the results in tabular form, PRINT statement is included in the input. General format is same as that of .PLOT except .PRINT instead of .PLOT.

. TRAN Statement : General form of this statement is

. TRAN TSTEP TSTOP <TSTART>

Example

.TRAN 1NS 100 NS

TSTEP is the printing or plotting increment for line-printer output of transient analysis. If TSTART is not defined its default value is 0. Results are plotted/printed for the time between TSTART to TSTOP.

Pulse input statement : General format

VXX N+ N- PULSE (V1 V2 TD TR TF PW PER)

Example VIN 3 0 PULSE (0 5 2NS 2NS 2NS 50NS 100NS)

V1 = Initial Value

V2 = Final value

TD = Initial delay

TR,TF = Rise time and fall time

PW = Pulse width

PER = Period of the pulse.

4.2 MOSFET MODEL DESCRIPTION [20-23]

SPICE 1L uses FROHMAN-GROVE model of MOSFET. This model requires typically 15 parameters to characterise the MOSFET behaviour. SPICE 2G uses three levels of MOSFET models. The first level MOSFET model describes a square-law I-V characteristic for MOSFET based on Shichman-Hodges model equations, second level MOSFET model is an analytical

model while third level model of MOSFET is a semiempirical model. Both MOS level 2 and level 3 include second order effects.

4.2.1 FROHMAN-GROVE MODEL : The D.C. characteristics of the MOSFET are determined by the parameters VTO, BETA, LAMBDA, PHI and GAMMA. VTO is zero bias threshold voltage of the device charge storage is modelled by three constant capacitances CGS, CGD and CGB. These capacitances are present there due to overlapping of the gate material on drain, source and bulk regions; by the nonlinear tgate channel distributed capacitance which is actually series combination of COX and nonlinear depletion capacitance of the channel, this capacitance is averaged and splitted into three average constant capacitances between gate drain, tgate source and gate bulk using J.E. Meyer formulation [21] ; by nonlinear depletion capacitance for both substrate junction which vary as -1/2 power of junction voltage and they are determined by parameters CBD, CBS and PB. PB is bulk junction potential. An equivalent circuit as the MOSGET is shown in Fig. 4.1. This circuit is directly derived from the knowledge of MOSFET geometry and physics of operation, the distributed capacitances have been represented by lumped capacitances. Nonlinear active gate-channel capacitance and depletion layer capacitances are shown by capacitor symbol enclosed in the rectangle.

For the purpose of computer-aided transient circuit analysis, it would be desirable that all of the above capacitances be constant. This approximation greatly simplifies the numerical analysis involved by eliminating the need to modify the companion model of capacitor at each time step. This can be done by averaging the capacitance value over the approximate expected voltage variation and this average value is substituted for each voltage dependent capacitance.

If it is assumed that the drain-substrate and source-substrate junction is a step junction then CBS and CBD are of the form,

$$CBS = A_S \left(\frac{qN_A \epsilon}{2}\right)^{1/2} (-V_{BS} + 2\phi_F)^{-1/2}$$

and

$$CBD = A_D \left(\frac{qN_A \epsilon}{2}\right)^{1/2} (-V_{BD} + 2\phi_F)^{-1/2}$$

where $2\phi_F$ is approximately equal to bulk junction potential PB. This expression should be averaged over the voltage variation yileidng

$$\bar{C}_* = 2A_* \left(\frac{qN_A \epsilon}{2}\right)^{1/2} [(-V_f+2\phi_F)^{1/2} - (-V_i+2\phi_F)^{1/2}]$$

where * = D for drain junction

= S for source junction

and $\epsilon = \epsilon_o \epsilon_s$

Constant values thus obtained will be used in computer program. Similarly active gate-channel capacitance of a MOSFET is the series combination of fixed gate oxide capacitance C_{OX} and the space-charge capacitance (depletion capacitance) $C_{space\text{-}charge}$ of the channel. This capacitance is distributed over the entire channel length. It must be split up into two lumped (nonlinear) capacitance CGD* and CGS*. This can be done by first finding the total gate charge.

$$Q_g = \int_0^L Q(y)dy = \int_0^L C_{OX} \quad V_{OX}(y)dy$$

where $V_{OX}(y)$ is surface potential at a point at a distance y from the source end. We may then define two lumped capacitances as

$$C_{GS} = \frac{\partial Q_g}{\partial V_{GS}} \quad ; \quad C_{GD} = \frac{\partial Q_g}{\partial V_{GD}}$$

The resulting relationship are

$$CGS = \frac{2}{3} C_{OX}\left[1 - \frac{(V_{GD} - V_t)^2}{(V_{GS}-V_t+V_{GD}-V_t)^2}\right]$$

$$CGD = \frac{2}{3} C_{OX}\left[1 - \frac{(V_{GS}-V_t)^2}{(V_{GS}-V_t+V_{GD}-V_t)^2}\right]$$

These capacitances are voltage dependent. A straight-line approximation for these capacitance variation is presented in Fig. 4.2.

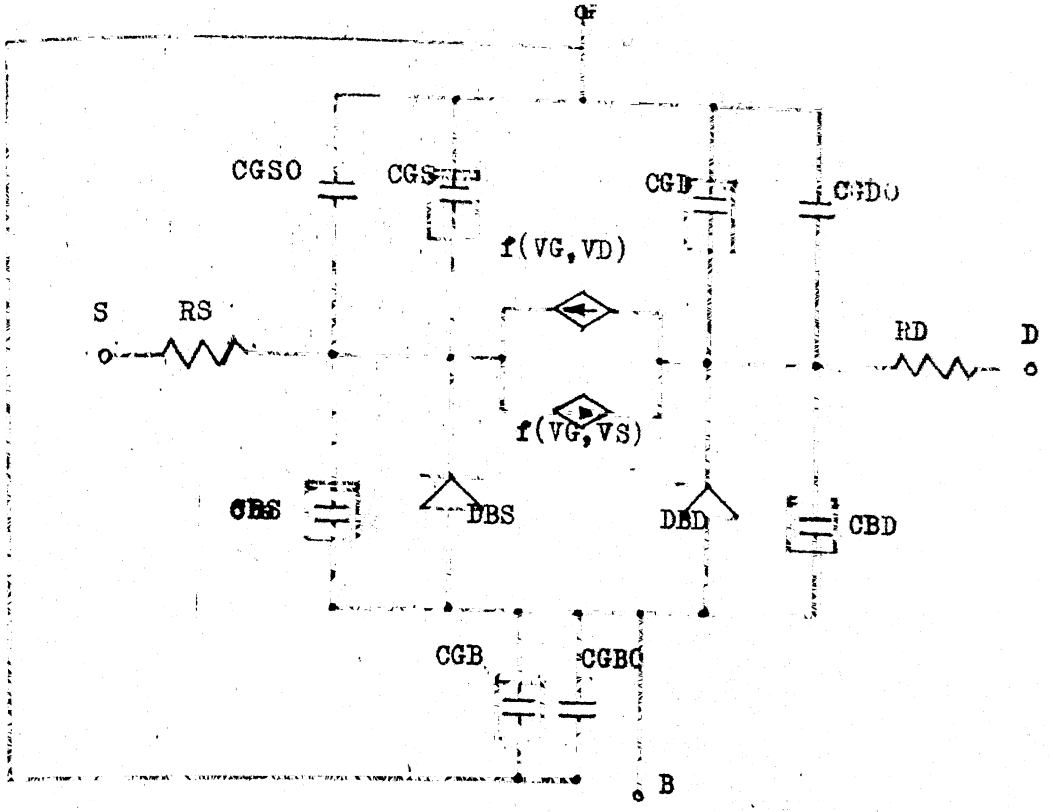


FIG.4.1EQUIVALANT CIRCUIT OF MOSFET

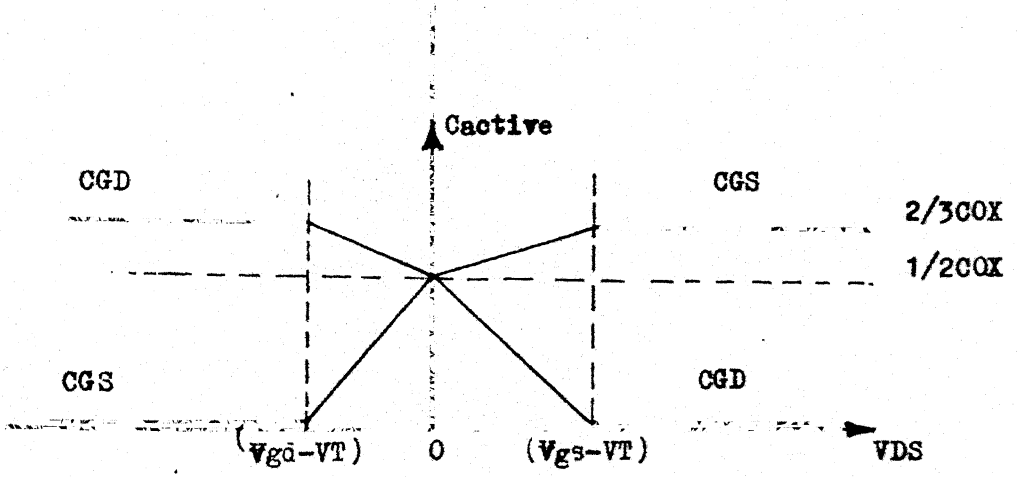


FIG 4.2 APPROXIMATE GATE & CHANNEL CAPANCITANCE VARIATION OF N-TYPE MOASFET

Some constant average value from the straight-line approximation is to used for computer simulation. Actual value to be chosen depends heavily upon how the device is expected to perform i.e. how its operating point will vary in the circuit. General practice is to take these capacitances as 1/2 C_{OX}.

The modified equivalent circuit of MOSFET, obtained by substituting all nonlinear voltage dependent capacitance by their average constant capacitance, is shown in Fig. 4.3. Two current sources are described by following equations.

$$f_1(V_G, V_S) = K_1 \begin{cases} 0 & V_{GS} < V_T \\ (V_{GS}-V_T)^2 & V_{GS} \geq V_T \end{cases}$$

$$f_2(V_G, V_D) = K_1 \begin{cases} 0 & V_{GD} < V_T \\ (V_{GD}-V_T)^2 & V_{GD} \geq V_T \end{cases}$$

and $$K_1 = \frac{\mu C_{OX}}{2} \frac{W}{L}$$

RD and RS are the resistance between ohmic contact and active region. Two diodes represent the P-N^+ junctions.

A summary of FROHMAN-GROVE model of MOSFET used in SPICE1L is given below.

1. VTO = Zero-bias threshold voltage

$$= \phi_{ms} + \left(-\frac{Q_{SS} - Q_{SD\ max}}{C_{OX}}\right) + 2\,\phi_f$$

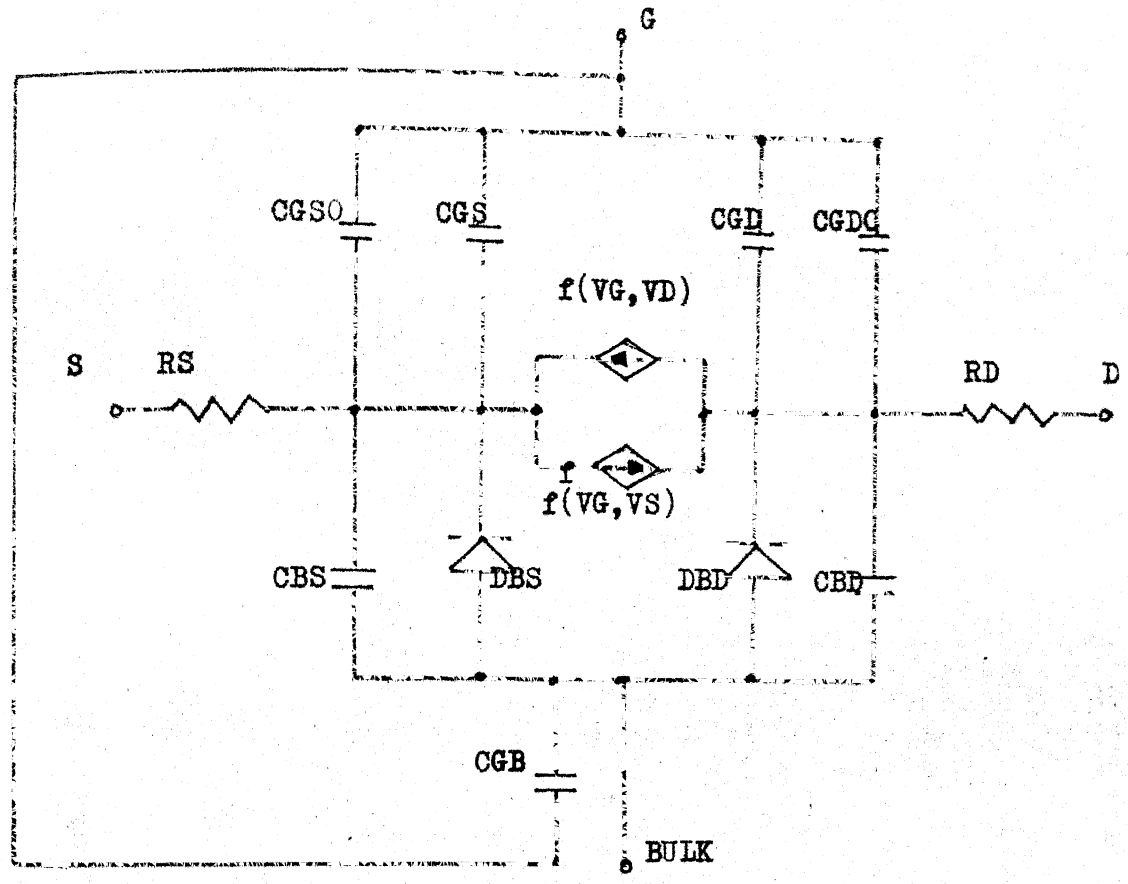


FIG.4.3 EQUIVALANT CIRCUIT OF MOSFET WITH CONSTANT CAPANCITANCES

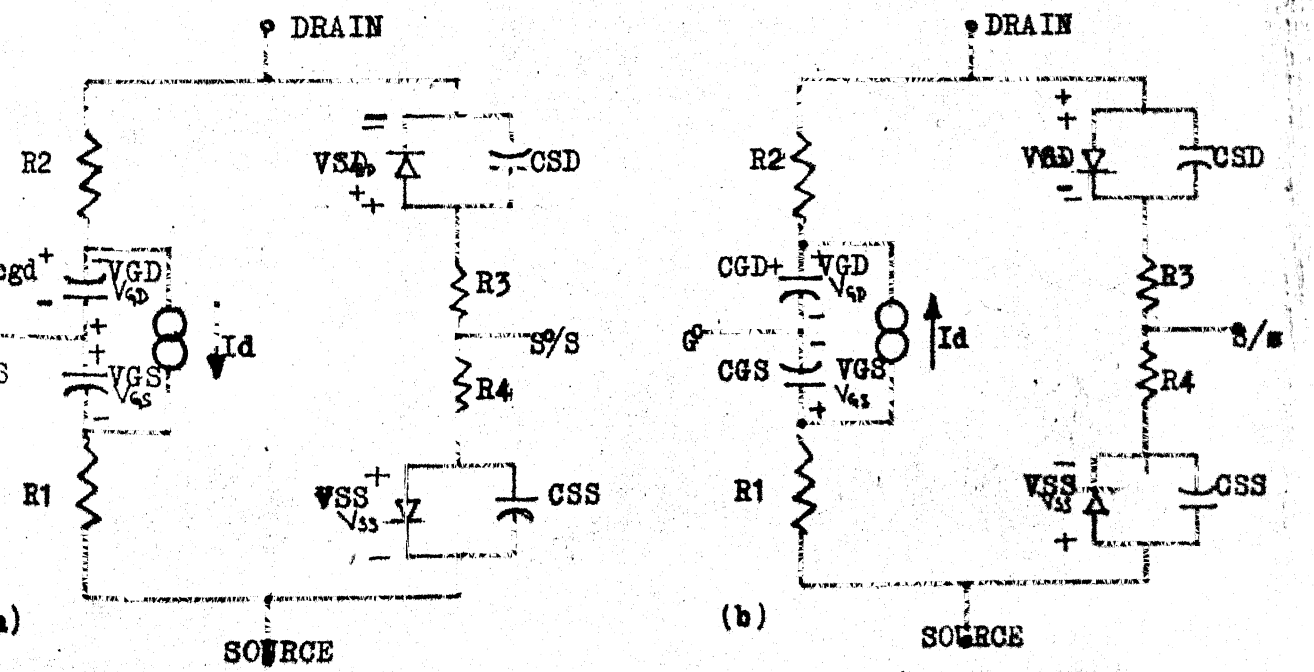


FIG 4.4 SH SCHICHMAN -HODGES MODEL FOR
(a) N CHANNEL (b) P CHANNEL

2. BETA = Transconductance parameter

$= \mu . C_{OX}$

3. GAMMA= Bulk threshold parameter,

$= (2 \epsilon q N_A)^{1/2} / C_{OX}$ where $\epsilon = \epsilon_o \epsilon_s$

4. PHI = Surface potential

$= 2\phi_F = \frac{2KT}{q} \ln(\frac{N_A}{n_i})$

5. LAMBDA = channel length modulation factor

= 0.0 to 0.02

6. RD = Drain diffusion region resistance

7. RS = Source diffusion region resistance

8. CGS = Gate-source overlap capacitance

9. CGD = Gate-drain overlap capacitance

10. CGB = Gate-bulk overlap capacitance

11. $CBD = \frac{2A_D[(qN_A)/2]^{1/2}}{(V_f - V_i)} [-(-V_f+2\phi_F)^{1/2} - (-V_i+2\phi_F)^{1/2}]$

12. $CBS = \frac{2A_S[(qN_A)/2]^{1/2}}{(V_f - V_i)} [(-V_f+2\phi_F)^{1/2} - (-V_i+2\phi_F)^{1/2}]$

13. PB = Bulk junction potential

$= \frac{KT}{q} \ln(\frac{N_D N_A}{n_i^2})$

14. IS = Saturation current of the junctions.

$$= Aq\, n_i^2 \left[\frac{D_n}{L_n}\,\frac{1}{N_A} + \frac{D_p}{L_p}\,\frac{1}{N_D}\right]$$

where D_n, L_n are the diffusion coefficient and diffusion length respectively.

4.2.2 Shichman-Hodges Model

It is a four terminal model. The effect of substrate bias on gate threshold voltage, channel length modulation effect on conductance of device in saturation have also been considered. It is applicable to both enhancement as well as depletion type devices. Equivalent circuits of MOSFET for N-channel and P-channel have been shown in Fig. 4.4. The equations relating I_D to the various voltages and material parameters are given as

$$V_T = V_{TO} + K_2[(-V_{BD}+2\phi_F)^{1/2} - (2\phi_F)^{1/2}]\big|_{V_{BD} > V_{BS}}$$

$$V_T = V_{TO} + K_2[(-V_{BS}+2\phi_F)^{1/2} - (2\phi_F)^{1/2}]\big|_{V_{BS} > V_{BD}}$$

where zero-bias threshold voltage, V_{TO} is given by

$$V_{TO} = \underbrace{(\phi_{ms} - \frac{Q_{SS}}{C_{OX}})}_{V_{FB}} + \underbrace{(2\phi_F - \frac{Q_{SD}}{C_{OX}})}_{\text{Due to band bending}}$$

Drain current, I_D

$$I_D = K_1(F_1-F_2)\ (1 + \lambda |V_{GS} - V_{GD}|)$$

where

$$F_1 = \begin{cases} 0 & V_{GS} < V_T \\ (V_{GS}-V_T)^2 & V_{GS} \geq V_T \end{cases}$$

$$F_2 = \begin{cases} 0 & V_{GD} < V_T \\ (V_{GD}-V_T)^2 & V_{GD} \geq V_T \end{cases}$$

$$K_1 = \frac{\mu\ C_{OX}}{2}\ \frac{W}{L} \quad ; \quad K_2 = \left(2 \epsilon\ q\ N\right)^{1/2} / C_{OX}$$

$$\epsilon = \epsilon_o\ \epsilon_s$$

Resistors R_1 and R_2 represent the series resistance between the ohmic contacts and the active region. R_3 and R_4 are the spreading resistances from source and drain junctions into the substrate region. CGS and CGD are constant capactiances representing the gate-channel capacitance. Value of CGS and CGD are chosen as one half of the gate oxide capacitance which is a fair approximation at small V_{DS}, as proposed by J.E. Meyer [ ]. Two diodes represent the two P-N junction between the drain and substrate and between source and substrate. CBD and CBS are two depletion capacitances associated with P-N junctions respectively. These capacitances are included in

the charge-control model of the P-N junction. Factor is taken to include channel length modulation in saturation region and K_2 is taken to include the body bias effect on threshold voltage. K_1 is simply gain factor. These equations are valid for both N-channel and P-channel over a voltage range which do not cause punch-through breakdown. This model has tobeen used in level 1 of the SPICE2G. User have option to use J.E. Meyer model or to use charge-control model to represent the active gate-channel capacitance. Field independent constant mobility is used. Narrow channel effect on threshold voltage is also not included. However, higher levels of model have provision to take these effects into account.

4.3 COMPUTER-AIDED MOSFET MODEL PARAMETER EVALUATION [11,20,24]

An interactive program has been developed to extract the MOSFET model parameter to be used in SPICE. Choice or correct and consistent set of model parameters for accurate simulation is very necessary. Generally the models used in the computer program are highly complex and the parameters of the model does not give a clear idea of their effect on device performance. Number of parameters to be specified is also generally large. To use such simulation program effectively, user has to study the device model first and then compute the related parameters using some engineering approximations. This is a very tedious job and it requires knowledge of physics of operation of the device. To facilitate the user, a program to

extract the model parameter has been developed. The program interactively calculates the various parameters using least of information provided by the user about actual physical geometry and processing of the device. After extracting the parameters it displays the resulting device MODEL description in a format acceptable to SPICE. If the generated model statement is not upto user's expectation, he has option to recalculate the model parameter with different inputs, otherwise he can save (store) this statement in a temporary file. As many model statements will be generated as many are required in the input SPICE program. After having all model-statements extracted, the program, on user's request, can substitute these statements in the main SPICE input program, execute the SPICE and then type the results on the terminal screen. The program has a modular structure and at present it can be used to extract parameters for FROHMAN-GROVE model of MOSFET. But it can be modified for other models. The program is of self explanatory type hence a condensed description has been given.

CHAPTER 5

CONCLUSION

The task of design of a complex LSI/VLSI systems of any kind can be broken into manageable small subtasks of cell design, with a well defined communication of the cell with others, in the system. Chip design can thus be decomposed geometrically and functionally. Interaction between the designs of two different cells should be as small as possible. Using the variety of cells, a library of standard cells similar to subroutine library can be built. If the designer needs, say, a delay flip-flop cell, he can select it from a library rather than construct it himself. Extensive use of standard cells or subcircuits in design of LSI/VLSI systems emphasizes the importance and necessity to pay attention to design of these cells or subcircuits. Poor design and performance of the cell itself may result in still poorer design and performance of the system using these cells.

In this thesis we have mainly concentrated on the complete design of such single cells or subcircuits from the specification of cell's function. An integrated approach to design of MOS circuits has been presented. A detailed description of MOS characteristic and concepts of MOS circuit design and analysis have been presented in Chapter 2. There we have included a computer program to perform the transient analysis of the MOS

circuits. The program allows depletion type transistors to be defined explicitly. It also calculate the VTO, BETA, GAMMA and other parameters of the model from process parameters.

Exclusive OR circuit cell is designed in random logic and it's layout schematic is prepared. For layout design, rules given by Mead and Canwey, have been referred. Similarly, to consider the structured logic design approach we have designed full-adder cell as PLA and its layout schematic is also prepared. To consider sequential logic design, we have designed a 4-bit variable modulo synchronous counter. Counter can be reset to any control-data input states. Layout schematic of the counter, represented by stick diagram is prepared. A two-phase ratioless dynamic shift register cell is designed to consider the dynamic logic design. Layout schematic for dynamic shift register cell is also prepared. Parasitic capacitance and resistance etc. are estimated from the detailed layout and device processing specifications, for each of the circuits. This step is a strong link between circuit design and process design to obtain required device characteristic. Using these estimated values of parasitics, circuits have been simulated using SPICE to verify their electrical functional specification. The simulated behaviour and output waveforms are quite encouraging and are close to our expectations. Smaller values of delays are obtained by careful placement of the transistor in the layout design. Since fabrication

facility is not available here therefore actual data on circuit performance is not given.

Concepts developed in this thesis can be directly extended to design of LSI systems. Design of larger circuits requires computer-aids and a dedicated large memory computer system with color graphics facility. It should be supported by various state-of-art simulation programs and design and verification tools. Successful completion of LSI system design projects, requires a joint effort by members of the design team and availability of above stated CAD tools. Therefore, future work as an extension of this thesis, should be planned keeping all these points into consideration.

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APPENDIX I

SIMIC

The input format is not a free format, however, fields on a line can be separated by comma or blank. All lines should start from first column. Program expects input data in several distinct groups. First line of each group provides the identification and size of that group.

I. Circuit description group

II. Output description and control group

III. Device model group.

[I] The first line in the input must be title of the circuit of length 50 characters, it will be printed as heading on each page of output file. The last line in the input file must be .END. Ground is always numbered '0'.

Voltage Sources : Two types of voltage sources are available. (a) A pulse, (b) Constant D.C.

SW N+ N- Initial value Find value Initial delay Final delay

All fields are essential.

Capacitors : Program accepts only constant and lumped capacitors. Floating capacitors are not allowed. General format is :

SN N+ N- Capacitance Value

MOSFETS : Unlike SPICE, the program allows user to define depletion type transistor. Threshold voltage can be adjusted by adding the equivalent implant charge to surface state density NSS. Some modifications in VT-model is necessary to include the PMOS. NDEV, NMAX are Number of active devices and maximum number of nodes respectively. General format is

SN MOSMP ND NG NS NS L W

MOSTYP is '1' for Enh. and '2' for dep. type device.

[II] Program plots the voltage waveform corresponding to any node in the circuit. The transient analysis step size information is also provided in the same line. For example

Output node TSTART TSTOP TSTEP

Choice of TSTEP is critical, it depends upon the minimum time constant of the circuit, typically TSTEP = 1 nanosec.

[III] General format is -

TEMP, NSSE, NSID, LAMBDA, TOX, NA, THETA,

whose TEMP is temperature at which simulation is required. NSSE, NSID are the surface state densities. LAMBDA is the parameter to model channel length reduction. TOX NA are the thickness of the gate oxide and substrate concentration respectively. MUE is the mobility of carriers in the channel and THETA is the parameter to model the effects of mobility variations.

Program Limitation

(1) At present program can handle at most 100 nodes.

(2) Maximum number of pulse input to the circuit may be 10.

(3) Only one output voltage waveform can be plotted at a time.